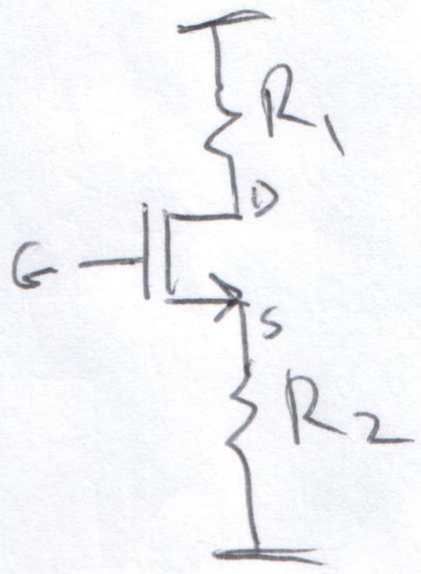
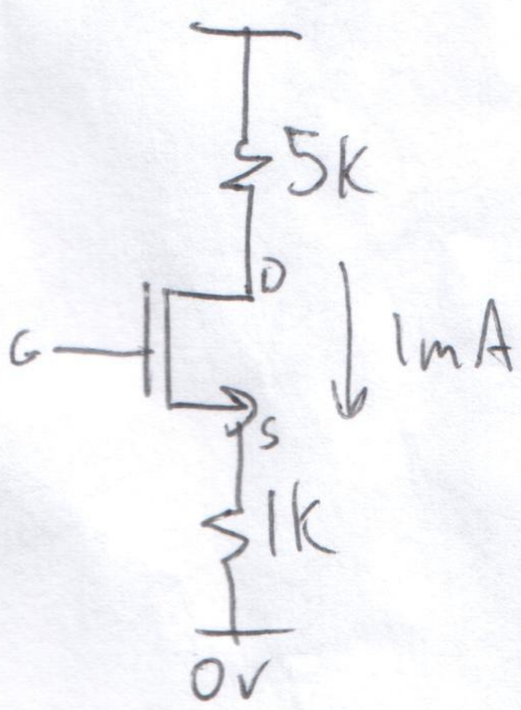


This circuit is very difficult to caluclate I_D from V_G because spurious quadratic roots are everywhere.

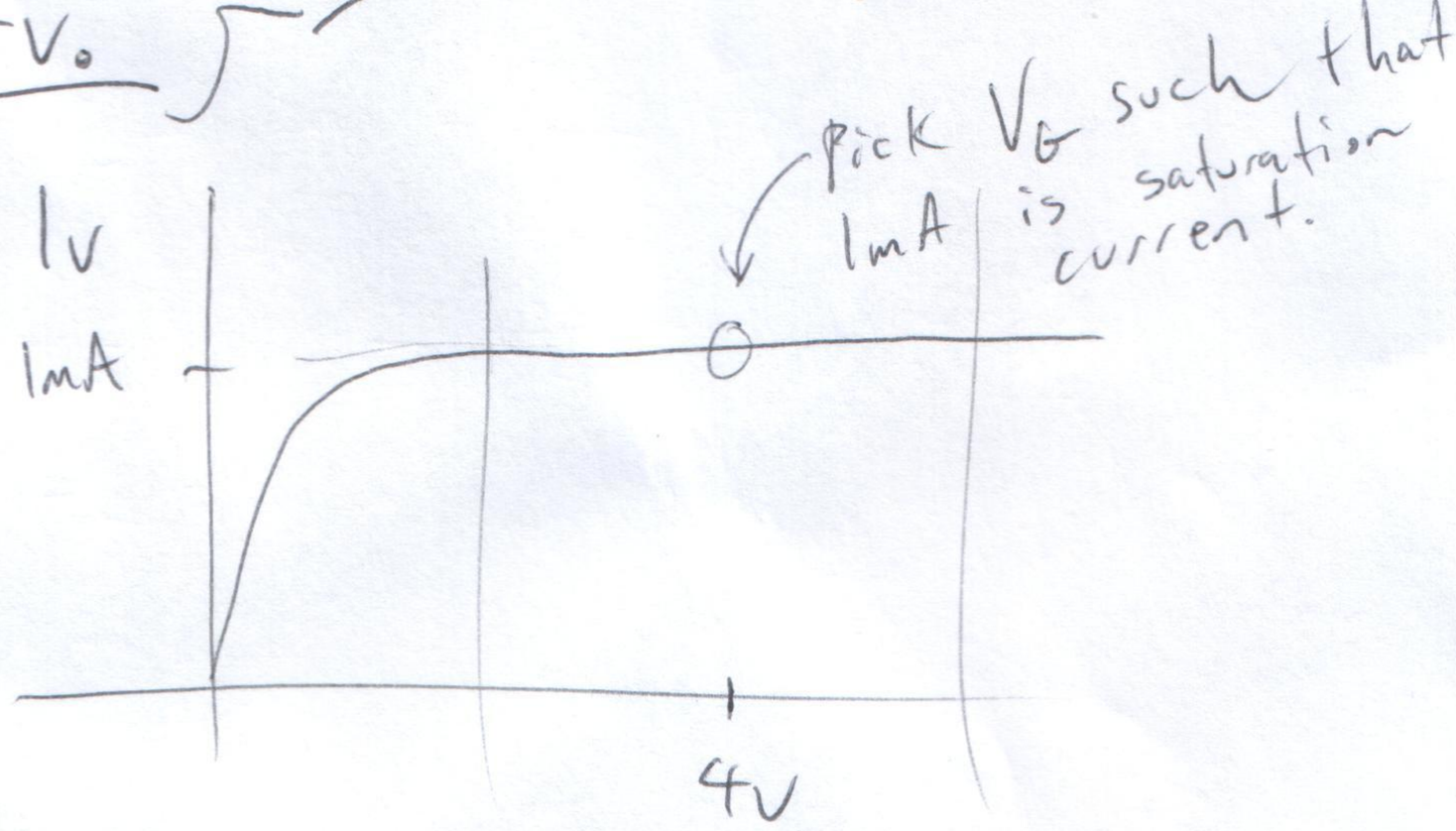
In practice this is almost never calculated without knowing something of the situation in advance.

Specifically, real circuit engineers have a plan.

$I_D = 1mA$
$V_{DS} = 4V$. ⟹ what is V_G?



$V_S = 1V$



$$I_D = K_n' \frac{W}{L} \left(V_{GS} - V_{TN}\right)^2$$

$$1mA = \underline{K_n' \frac{W}{L}} \left(\underline{V_{GS}} - 1\right)^2$$

Notice, we can set this with either of these.

→ In fact: Pick V_{GS}. $V_{GS} = 5V$.

$$K_n \frac{W}{L} = \frac{1}{16} mA$$

if $K_n' = 60 \mu A/V^2$,

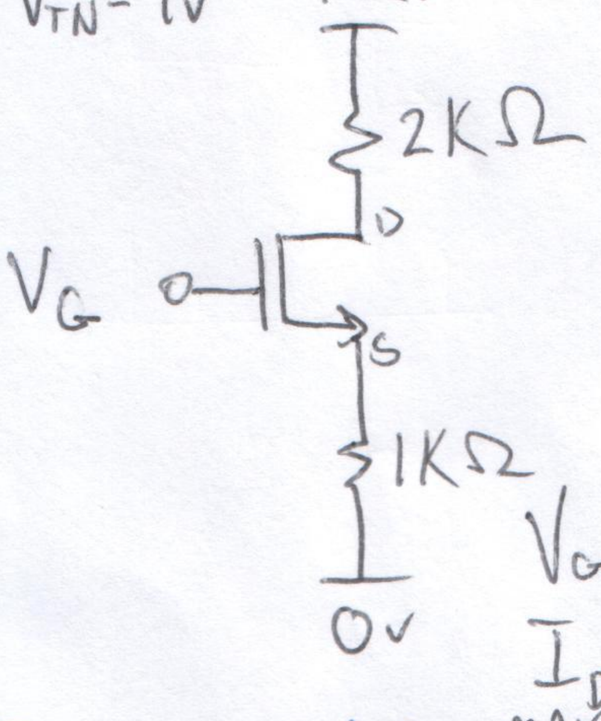
$$\frac{W}{L} = 625/1$$

sounds pretty rough, but really happens!

$K_n = 10\mu A/V^2$

$W/L = 10$

$V_{TN} = 1v$



$V_G = 5v$: Solve... But don't get stuck in a forest of spurious quadratic roots! (or at least learn something!)

All values of V_{GS} have a max current, set by V_{GS} @ Sat. Find that for some values of V_{GS}:

V_{GS}	1.5	2	2.5	3	3.5	4	4.5	5
I_D MAX	12μA	50μA	112.5μA	200μA	312μA	450μA	612μA	800μA

$I_{DSAT} = 100\mu A \frac{1}{2}(V_{GS} - V_{TN})^2$

(eight values is probably excessive, but can be handy.)
(and it's easy with MatLab/Octave/etc)

$V_{DS} = 12 - I_D \cdot 3K$

V_{DS} (at sat)	12.96	11.85	11.66	11.4	11.1	10.65	10.16	9.6

V_{DS} @ $V_{GS}=5$
Note: Definitely nowhere near linear.

now let's calculate V_G By $V_G = I_D \cdot 1K + V_{GS}$

1.51	2.05	2.61	3.2	3.8	4.45	5.11	5.8

actual value of circuit current probably about there.

Now you calculate, with a fairly good grip on what answer you should get.

$I_D = 50\mu(5 - V_S - V_{TN})^2$ $\quad V_S = 1K \cdot I_D$

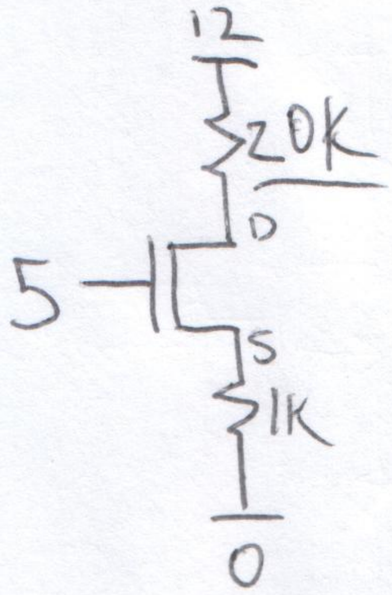
450μA	612μA

583μA OR 27mA

NOPE

Yep!

But what if it ended up linear.



V_{GS}	1.5	2	2.5	3	3.5	4	4.5	5
I_D MAX	12μA	50μA	112.5μA	200μA	312μA	450μA	612μA	800μA

These don't change because V_G is the same and so is the trans.

V_{DS} (at sat) [$V_{DS} = 12 - I_D \cdot 20K$]

V_{DS} (sat)	11.7	10.9	9.6	7.8	5.43	2.55	-.86	-4.8

$V_{GS} - V_{TN} < V_{TN}$ Saturation Can't Be Valid Here

$V_G = I_D \cdot 1K + V_{GS}$

V_G	1.51	2.05	2.61	3.2	3.8	X

NOT AVAILABLE

We've learned from this that if $V_{GS} > 3.5$, it's probably linear, and further that V_{GS} almost certainly is.

So: Linear:

$$I_D = 100\mu\left(5 - V_S - V_{TN} - \frac{V_D - V_S}{2}\right)(V_D - V_S)$$

$V_D = 12 - 20K I_D \quad V_S = I_D \cdot 1K$

$$I_D = 100\mu\left(4 - I_D \cdot 1K - \frac{12 - 21K I_D}{2}\right)(12 - 21K I_D)$$

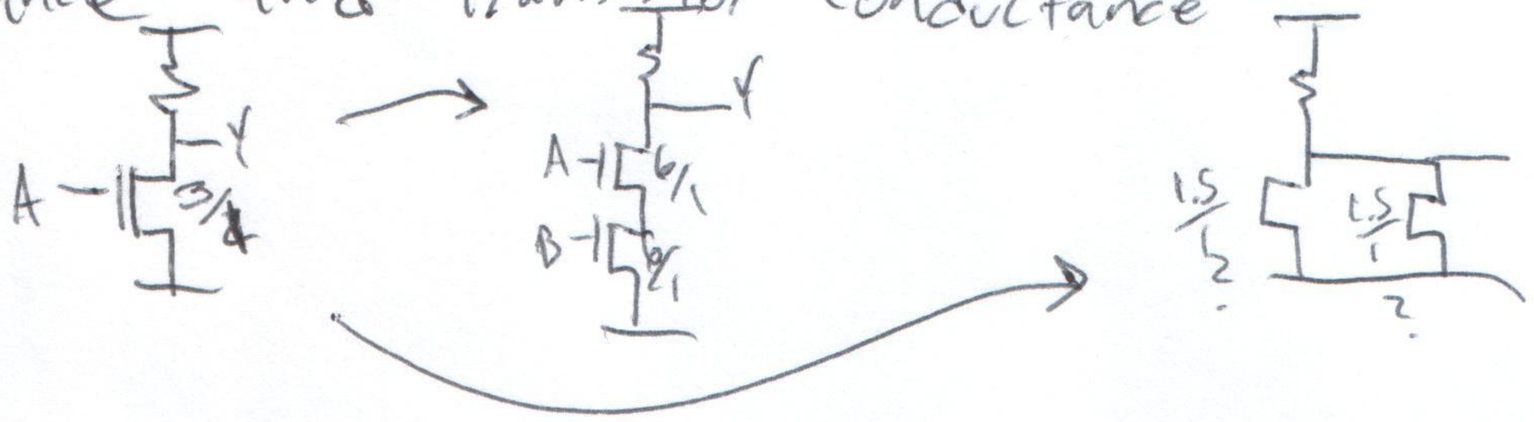
$$I_D = 100\mu(-2 + 10.5K I_D)(12 - 21K I_D)$$

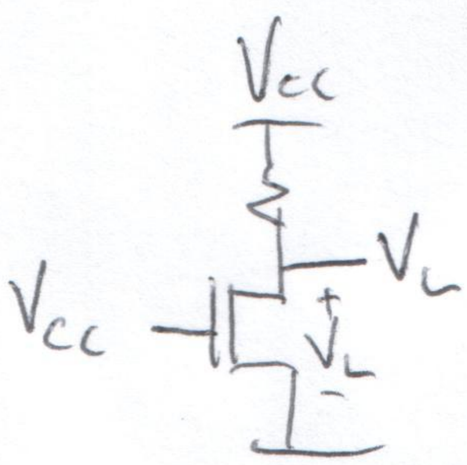
⇓

218μA OR 498μA

Both potentially valid. Iterate between V_G & I_D to be sure.

Resistance and Transistor "Conductance"



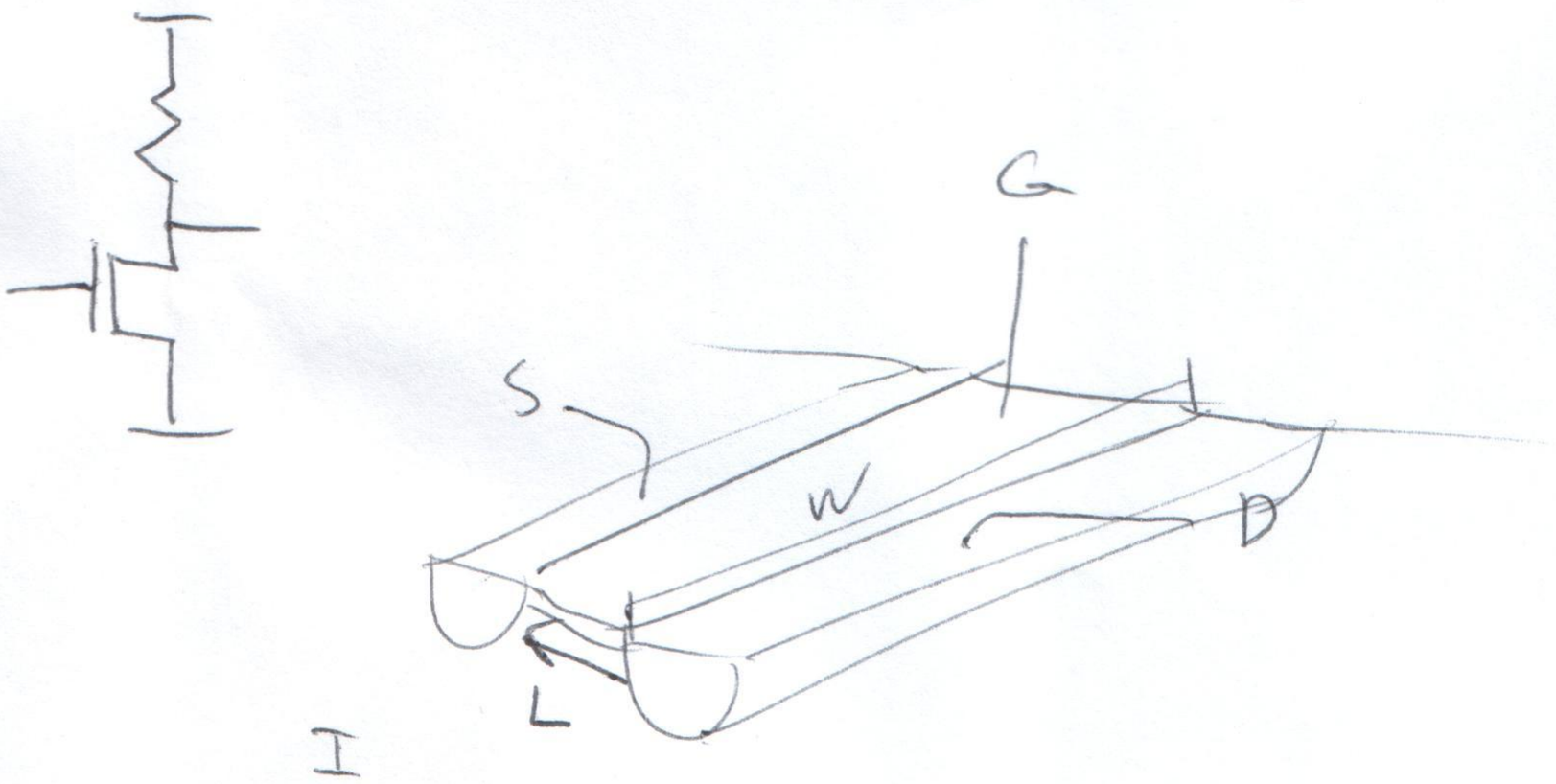


$$I_D = \underbrace{\frac{V_{CC}-V_L}{R} = k_n' \frac{W}{L}\left(V_{GS}-V_{TN}-\frac{V_L}{2}\right)V_L}_{\text{Solve this monstrosity}}$$

$$V_{CC}-V_L = \underbrace{k_n' \frac{W}{L} \cdot R}\left(V_{GS}-V_{TN}-\frac{V_L}{2}\right)V_L$$

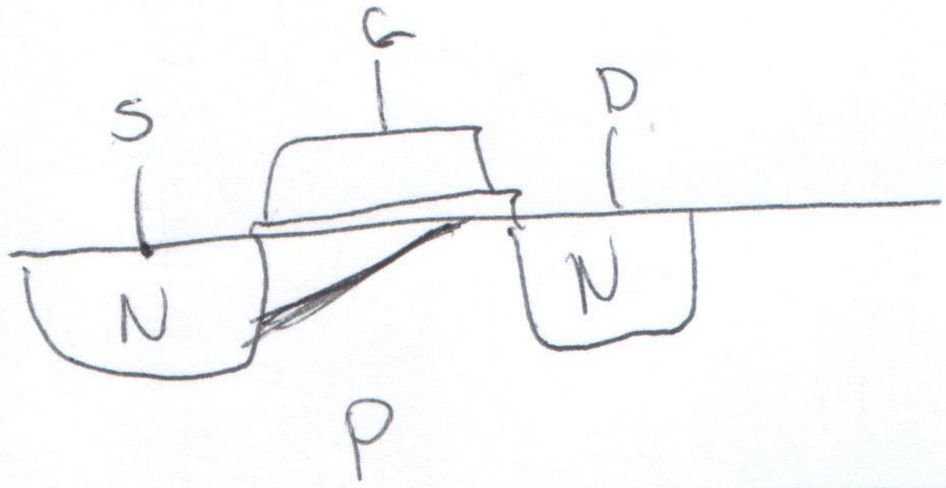
$$\underbrace{k_n' \frac{W}{L} \cdot R}_{\text{conductive}} = \underbrace{\frac{V_{CC}-V_L}{\left(V_{CC}-V_{TN}-V_L/2\right)V_L}}_{\text{resistive}}$$

↑ Dimensionless-ish wad of voltages



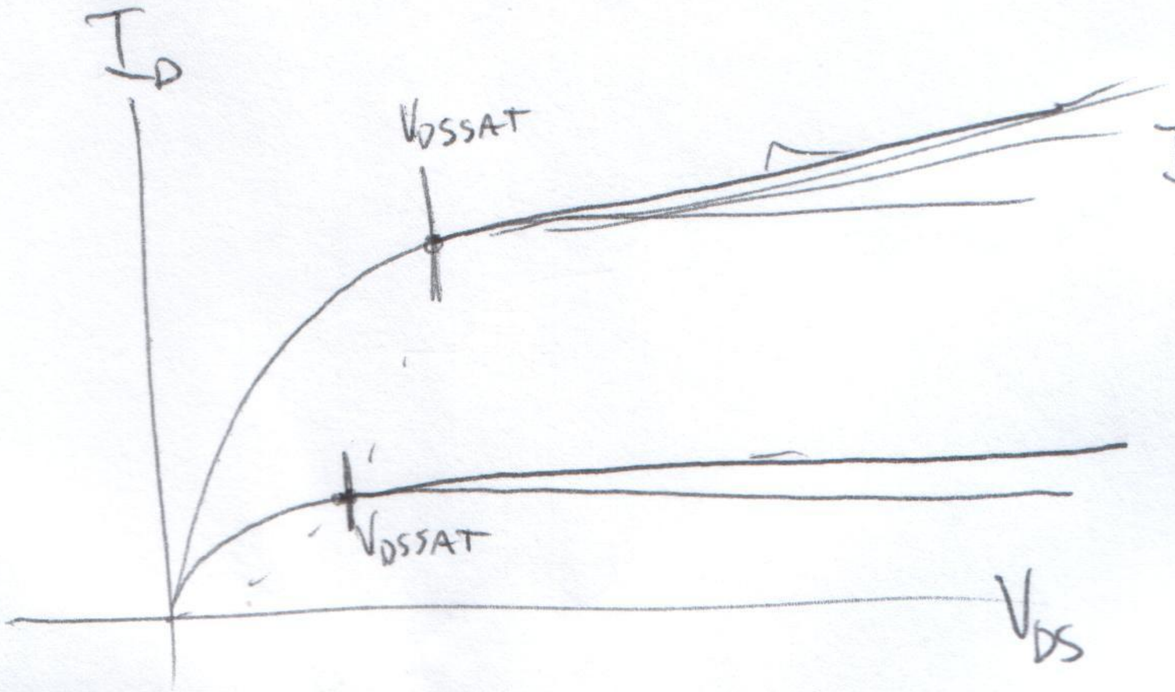
I

Impact of Channel Width Modulation



V_{DS} → bigger

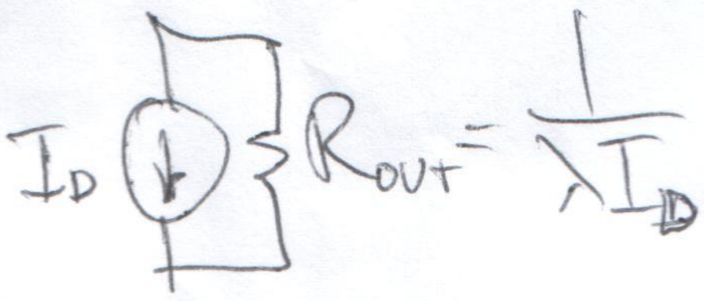
Conductivity in channel → higher

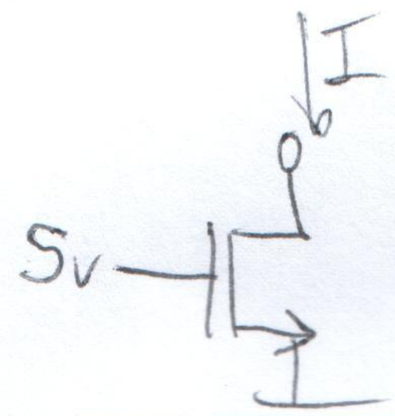


$$I_D' = I_D\left(1 + \lambda\left(V_{DS} - V_{DSSAT}\right)\right)$$

$$V_{DSSAT} = V_{GS} - V_{TH}$$

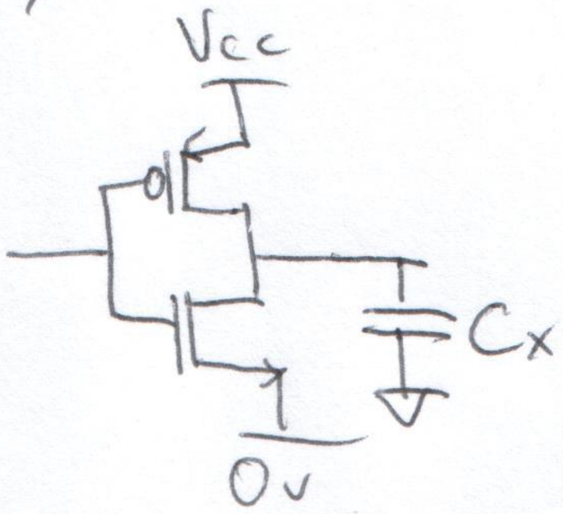
from inequality

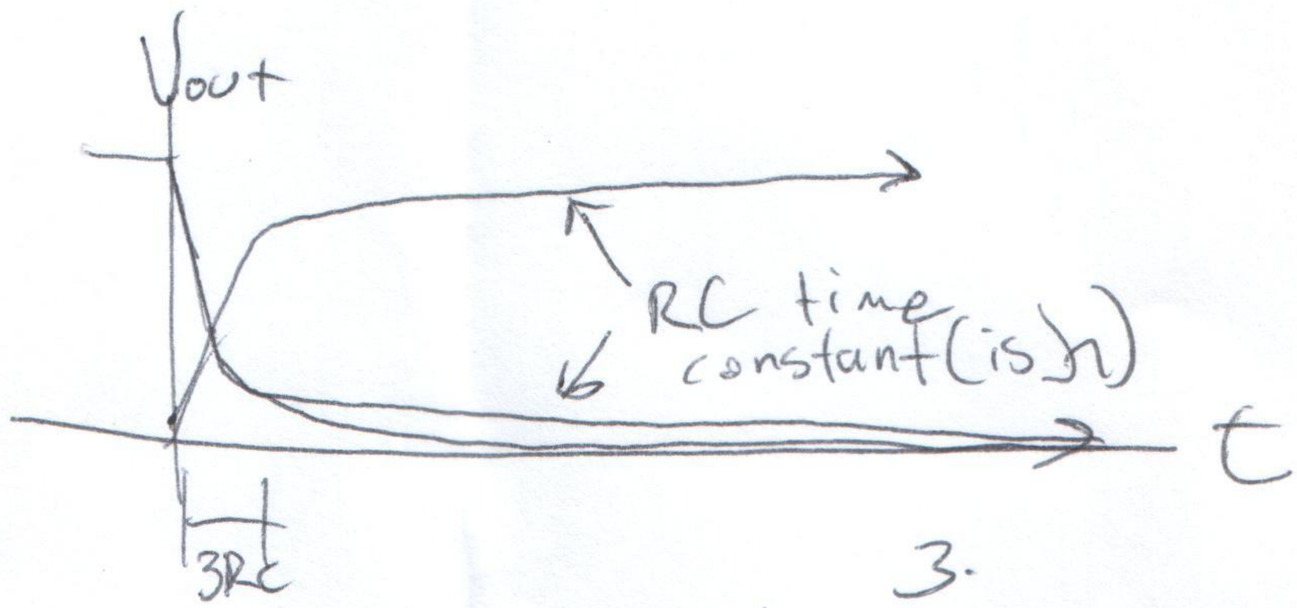




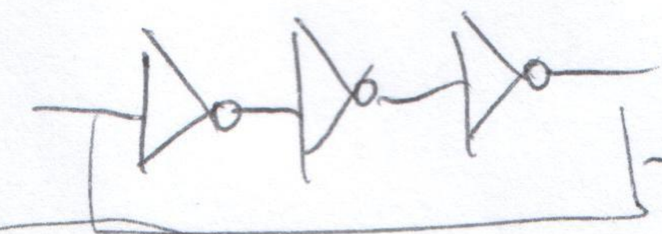
Current source no longer ideal.

Delay & Gates:



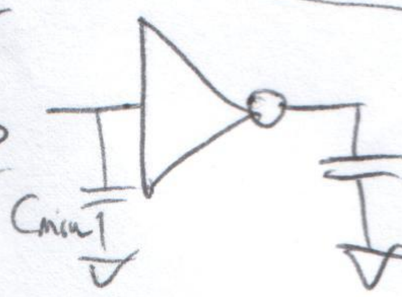


T_{Delay} = lots of things, let's go with ~~4~~ R-C

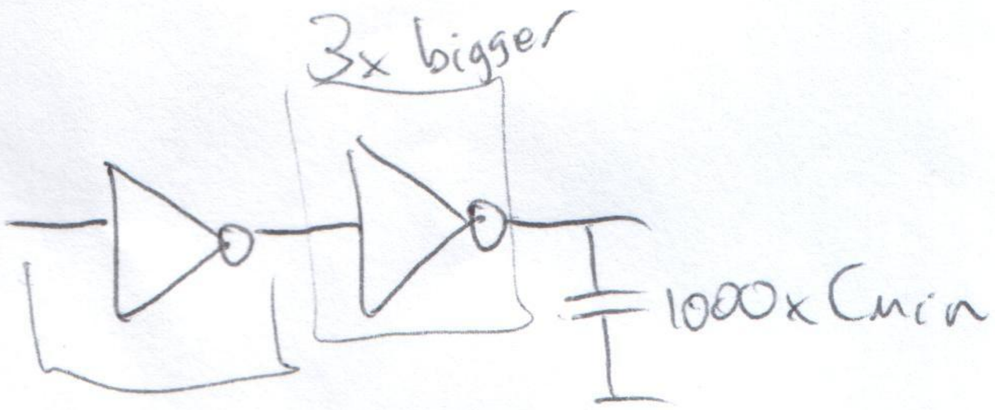


$\rightarrow 3 \times T_{Delay}$] not exactly accurate

Buffer chains

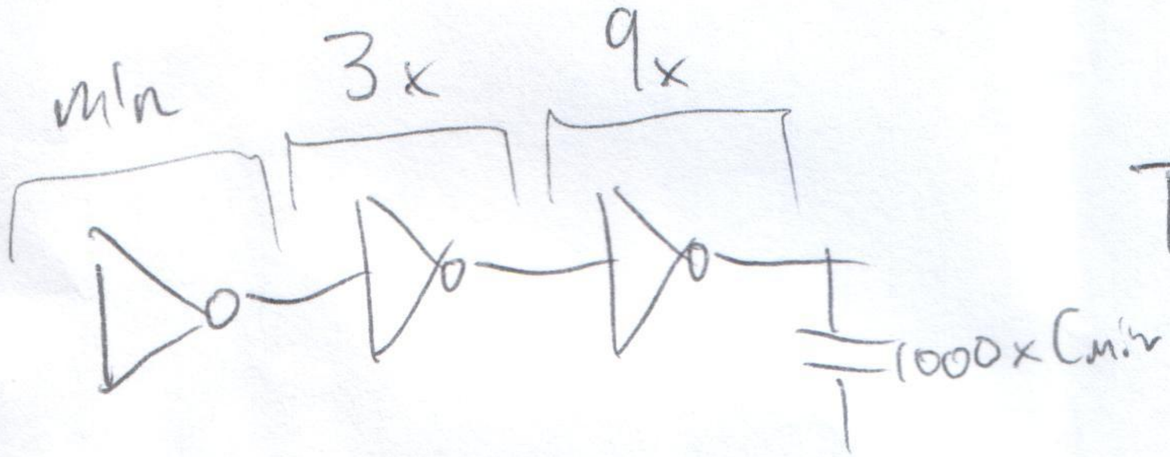


$\longrightarrow T_{Delay}' = \underline{1000 \times T_{Delay}}$



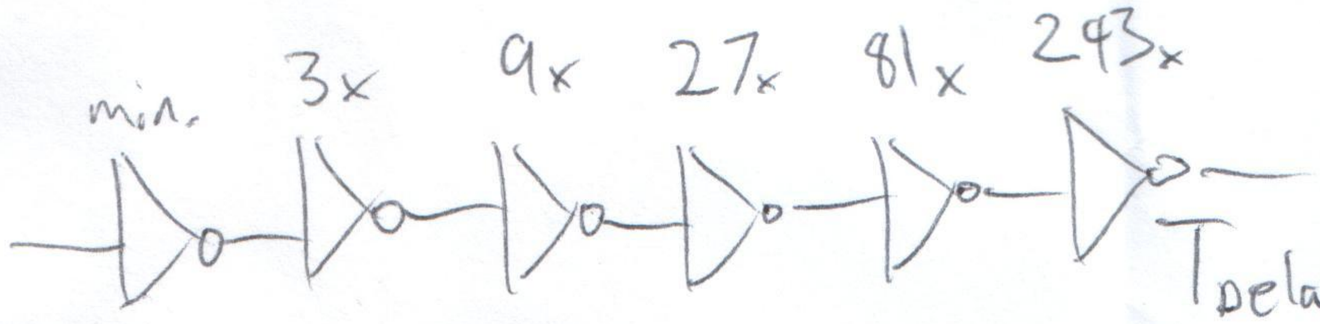
$T_{Delay}' = 3 \times T_{pelay} + \frac{1000}{3} T_{pelay}$

$\simeq 336 \times T_{pelay}$



$T_{pelay}' = 3 \times T_{pelay} + 3 \times T_{pelay} + \frac{1000}{9} T_{pelay}$

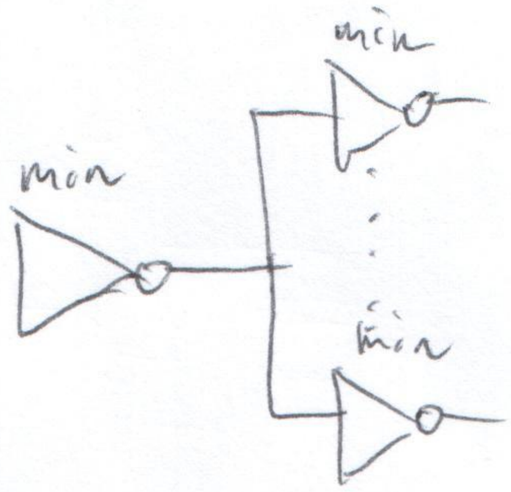
$\simeq 117 \times T_{pelay}$



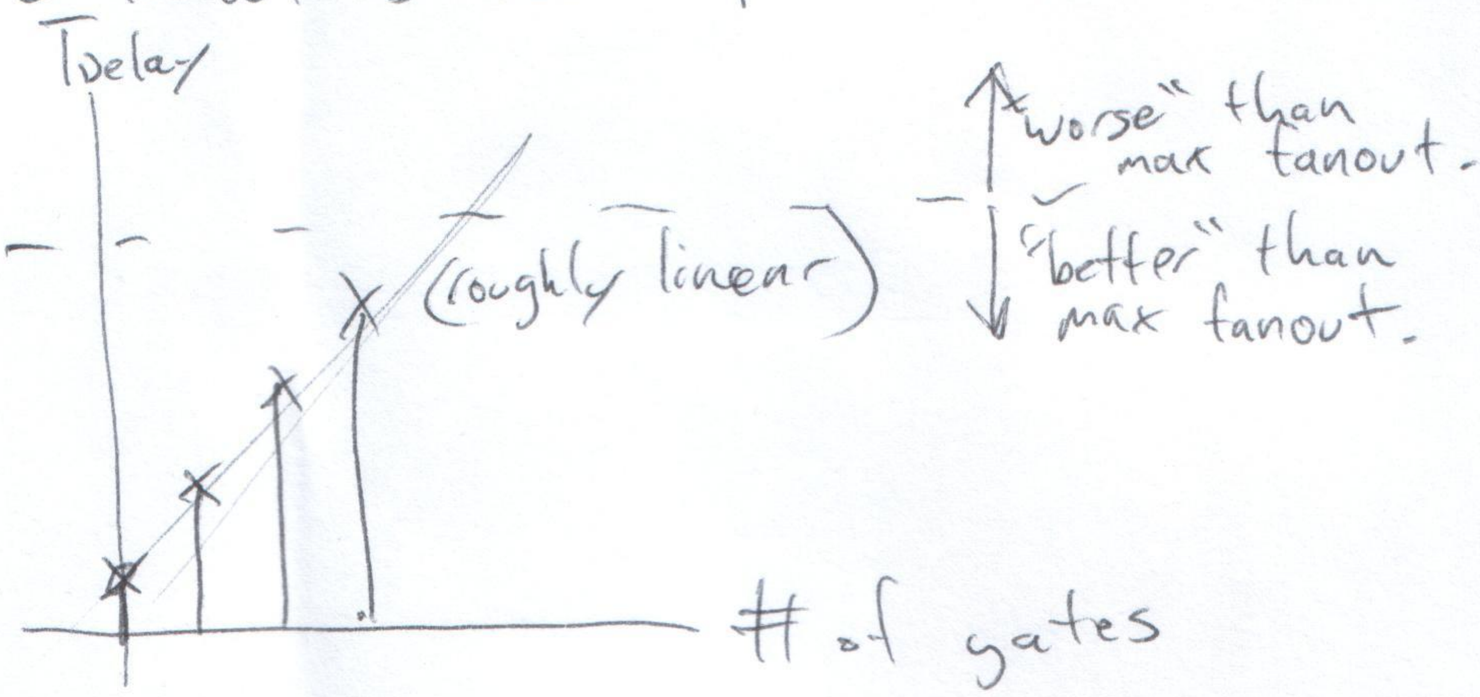
$T_{Delay}' = 15 \times T_{pelay} + \frac{1000}{243}$

$\underline{\simeq 20 \times T_{Delay}}$

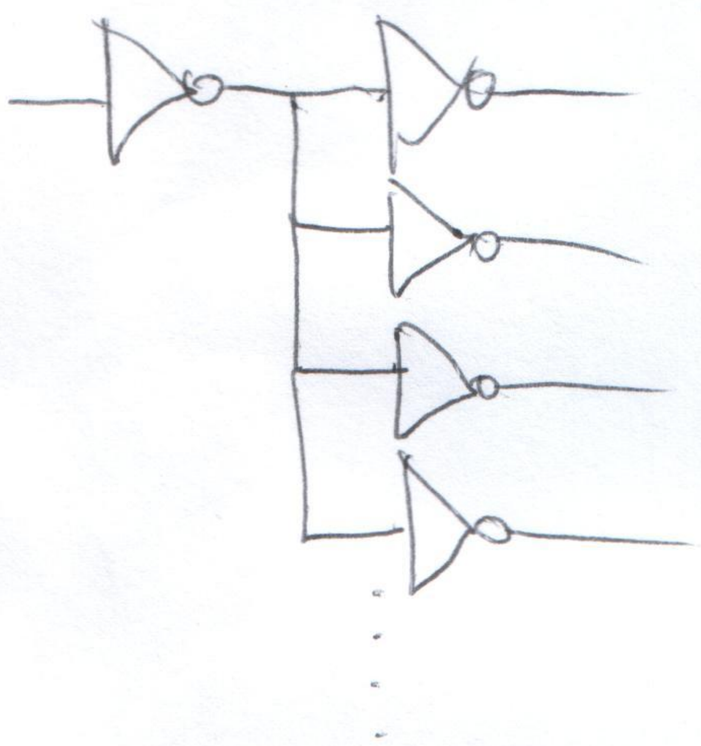
Related: Fanout



Gate fanout is not a precise science.



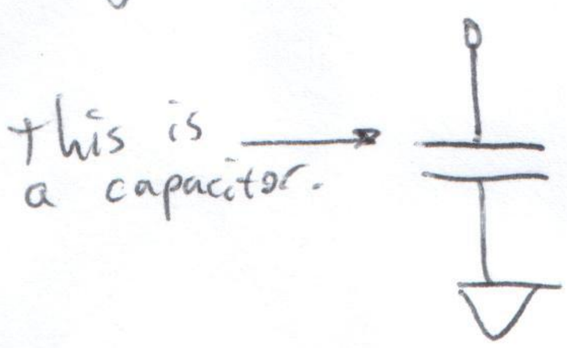
This distinction has more to do with what we just talked about:

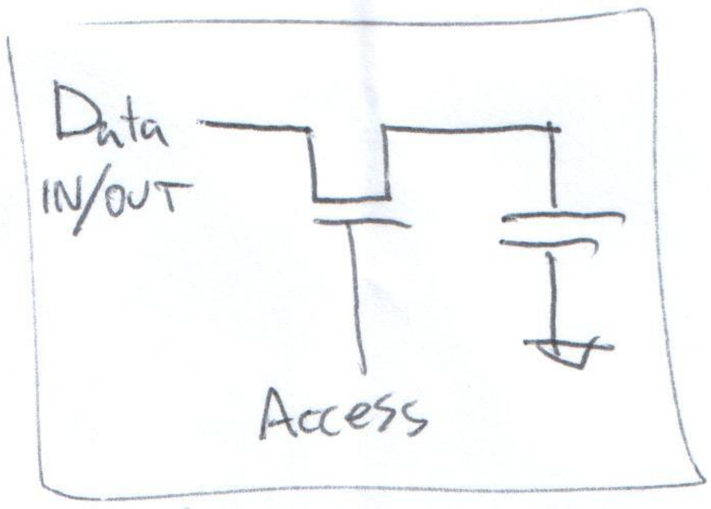


at what point does it start to make more sense to buffer a logic stage?

"Fun" fact: it's possible to tune every gate in a system to have close to the same RC constant by sizing everything and/or buffering. Some chips might even do this for super-high-speed logic.

Storage.





this is a DRAM cell

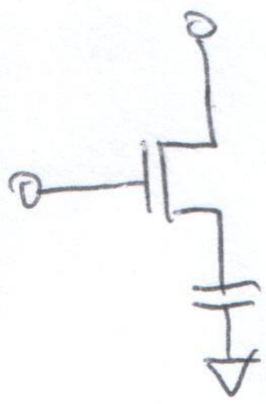
Body Effect

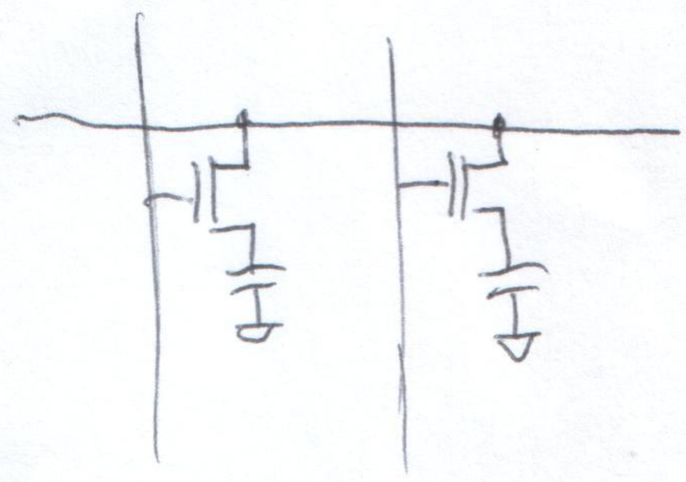
$$V_{TB} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\psi_B} - \sqrt{2\psi_B}\right)$$

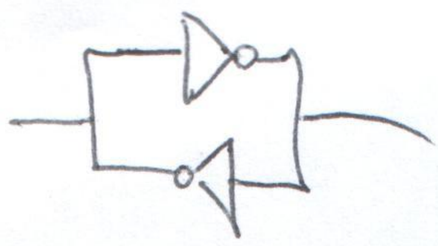
γ: mod. param.

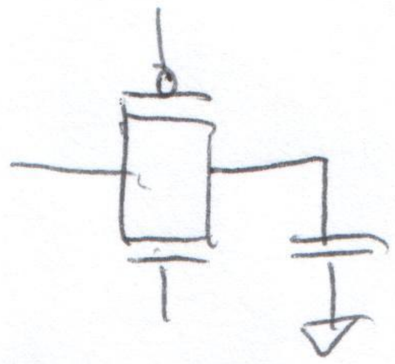
$V_{BUILT-IN}$

wow, that's awful....

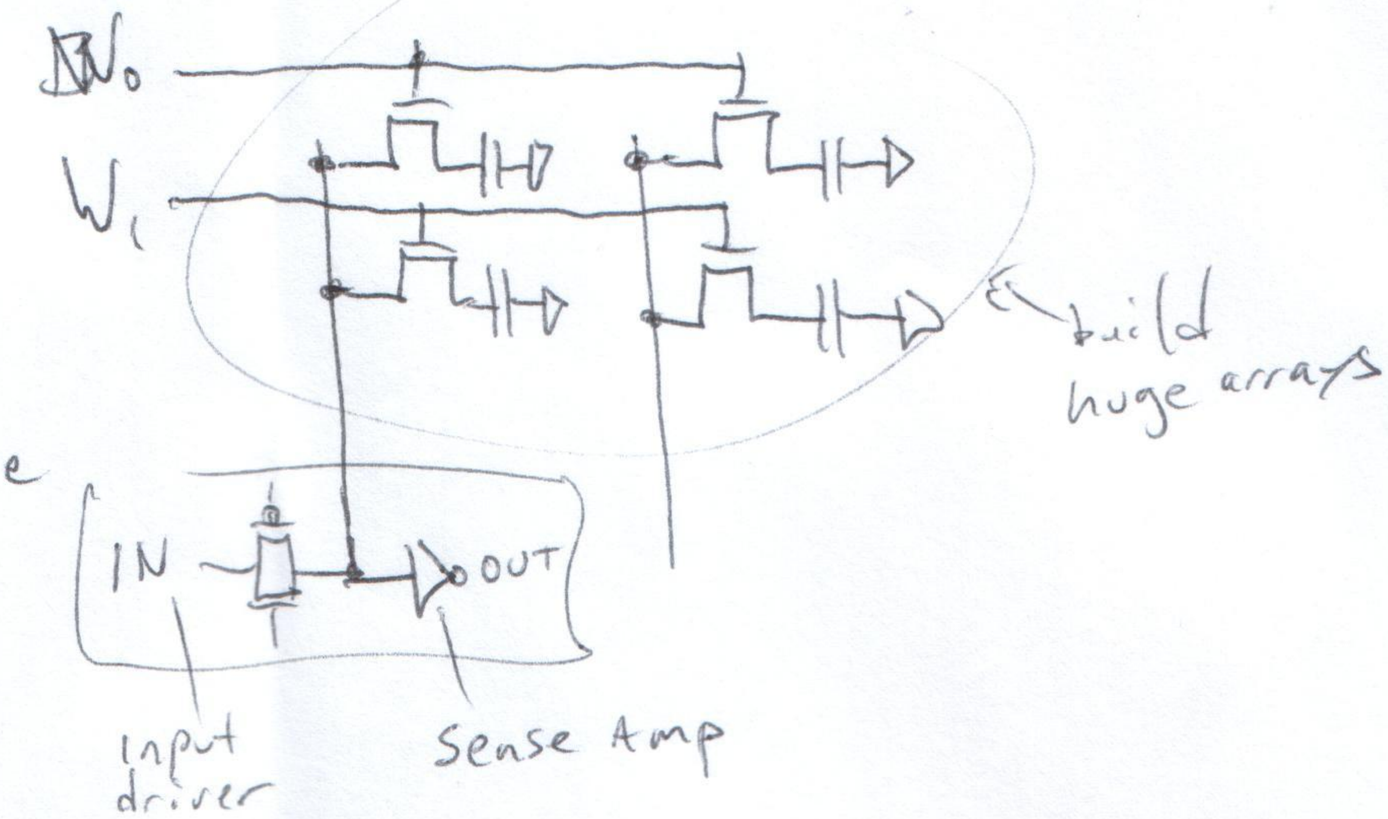




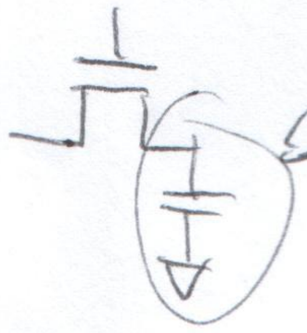




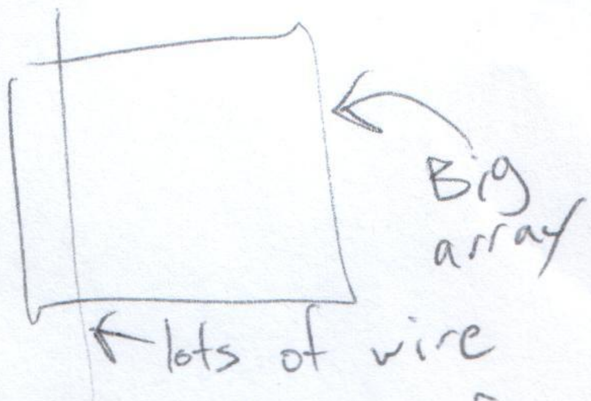
V_{out} -could- do this,
but that would require
2 transistors.



Problem:

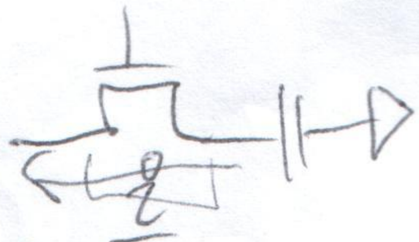


Not a giant capacitor.



Reading costs charge, so reload after you read!

Also:



NOT a perfect open circuit.

current will leak out quickly!

solution?!
Literally just read all the cells and reload every so often

(I am not kidding.)