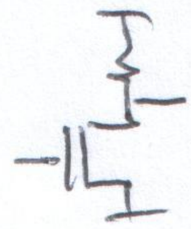
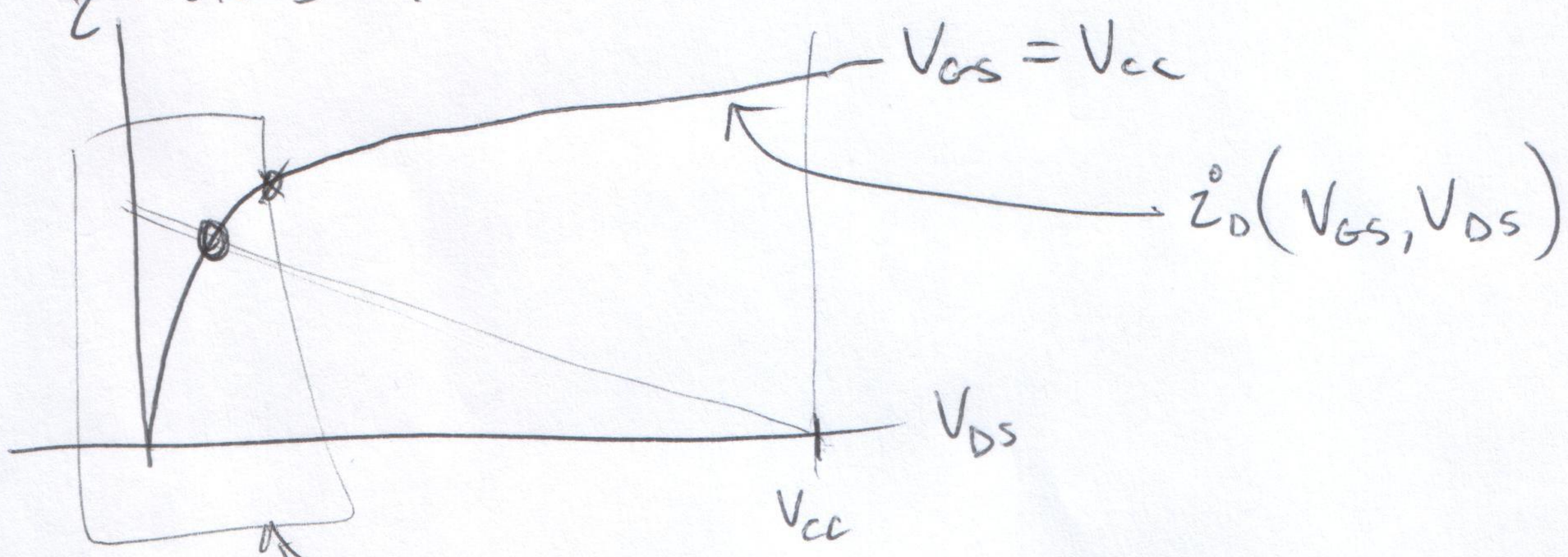
R_{on} & Gates:



Picking W/L



for a good inverter, i_D° in linear range

R:

$$i^\circ \cdot R = V_{CC} - V_{DS}$$

M_1:

$$i_D^\circ = K_n' \frac{W}{L}\left(V_{CC} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$$

✱ Pick a value of V_{DS} $[V_{DS} = V_L]$

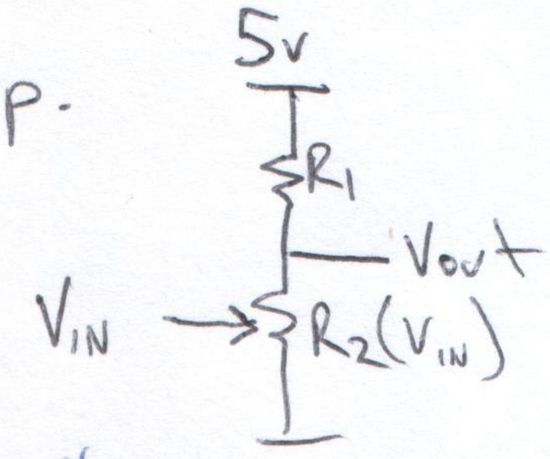
✱ set $\frac{V_{CC} - V_{DS}}{R} = K_n' \frac{W}{L}\left(V_{CC} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$

$$\left[\frac{W}{L}\right] \cdot [R] = \frac{V_{CC} - V_{DS}}{K_n'\left(V_{CC} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}}$$

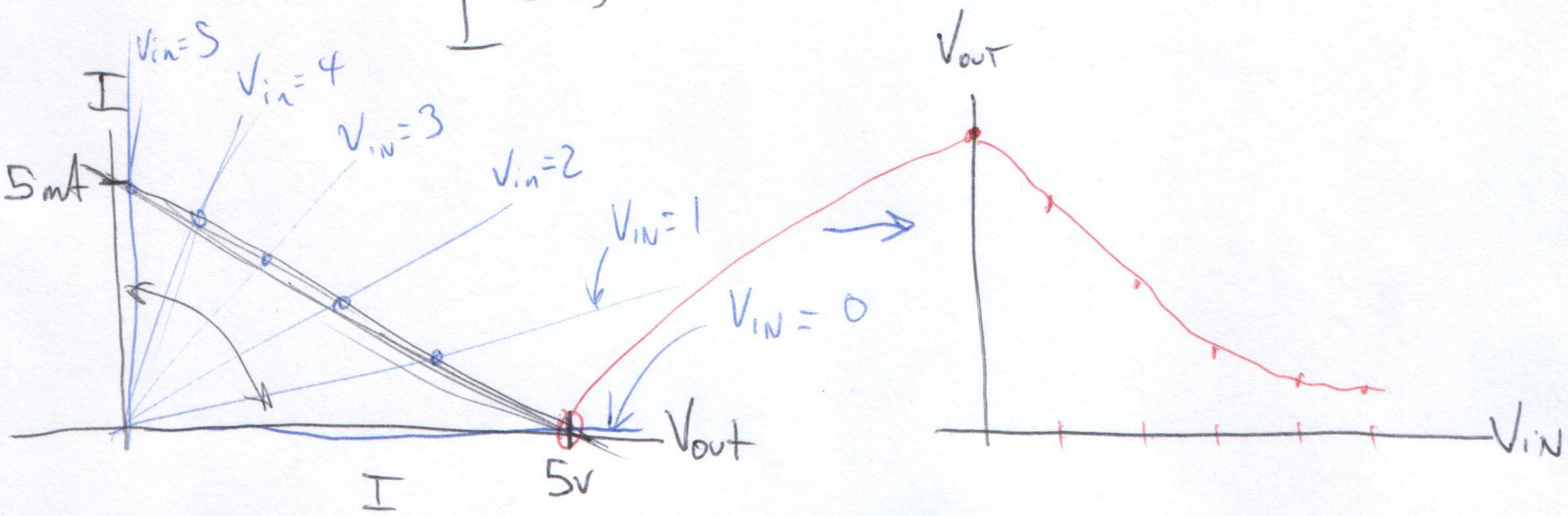
---

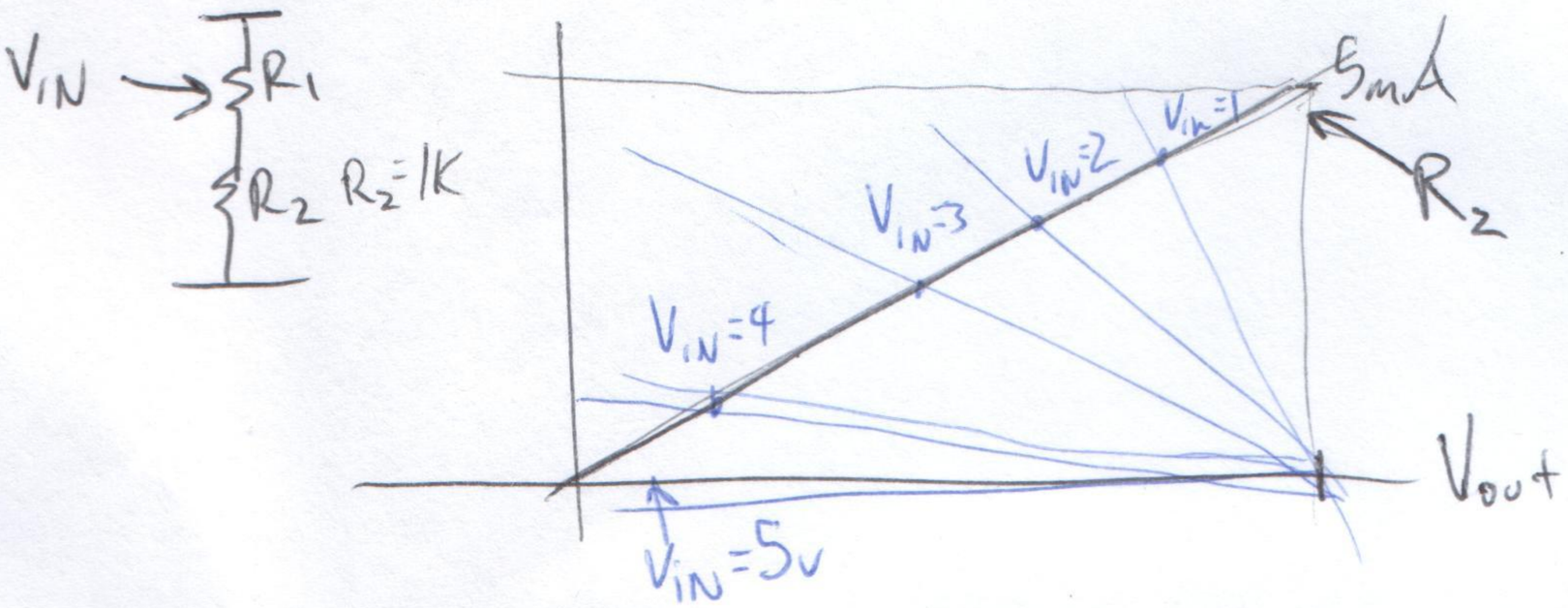
for a chosen value of V_{CC}/V_{DS}, $\frac{W}{L}$ or R determine each other.

The Warmup.

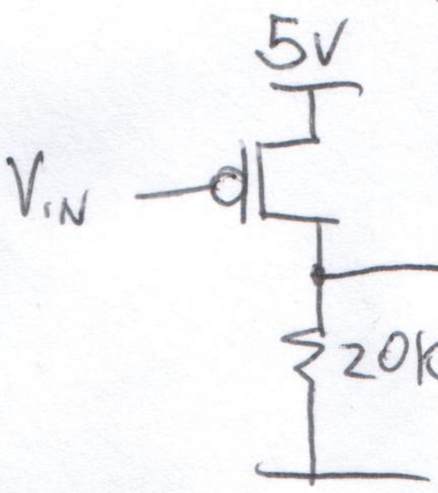


$R_1 = 1K$





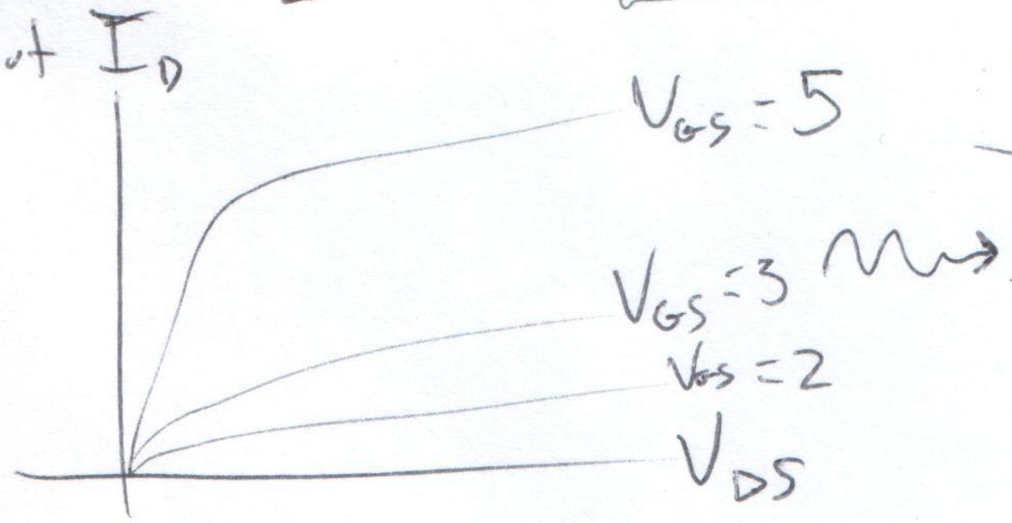
What we did yesterday:

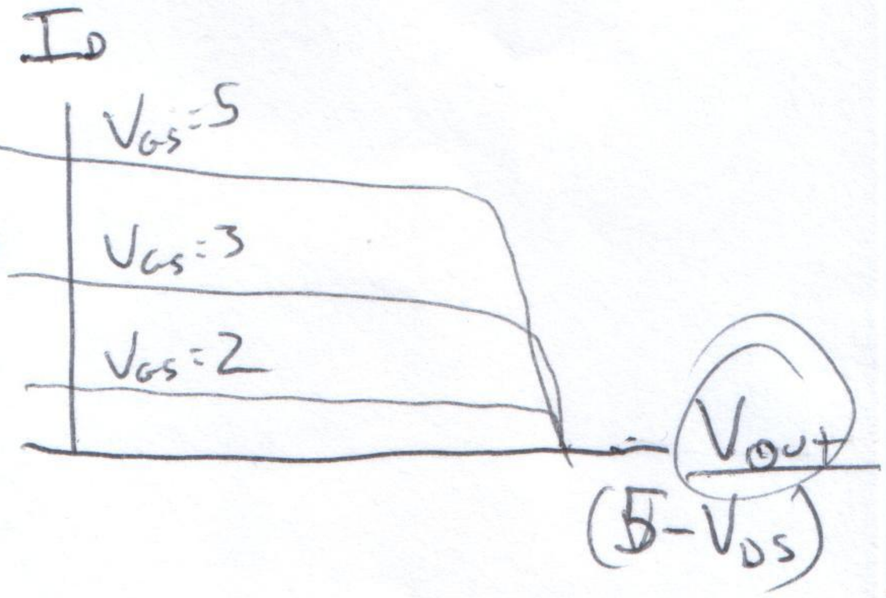


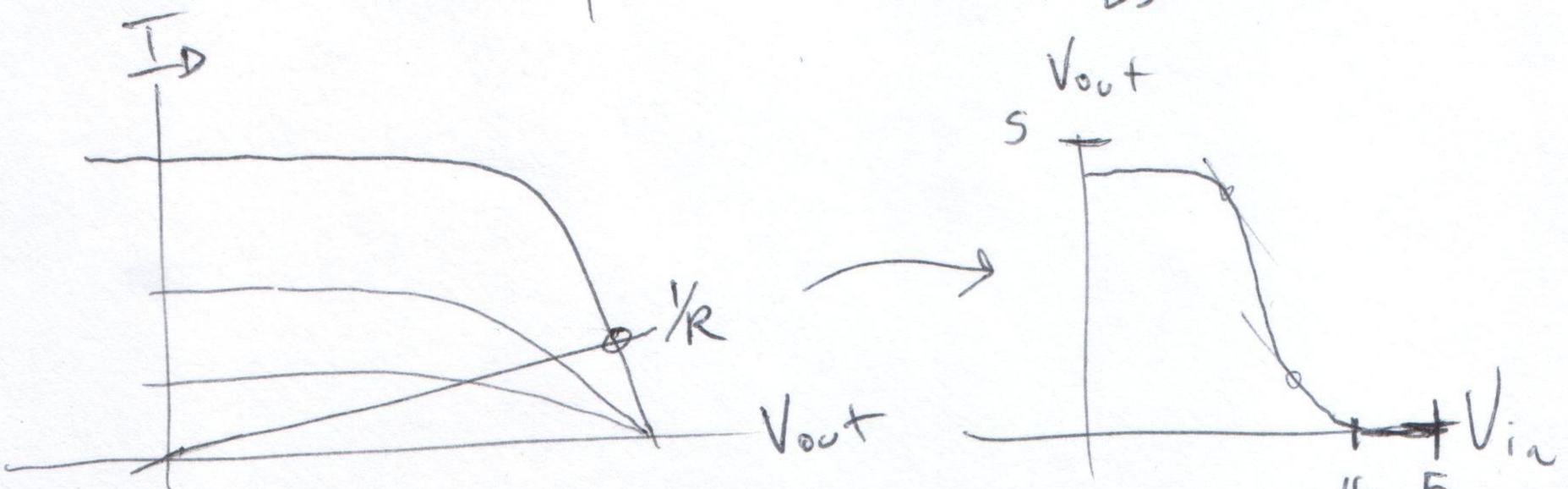
~~$K_p' = 10\mu A/V^2$~~
~~$\frac{W}{L} = 10$~~

$K_p' = 5\mu A/V^2$
$\frac{W}{L} = 20, V_{TP} = 1v$

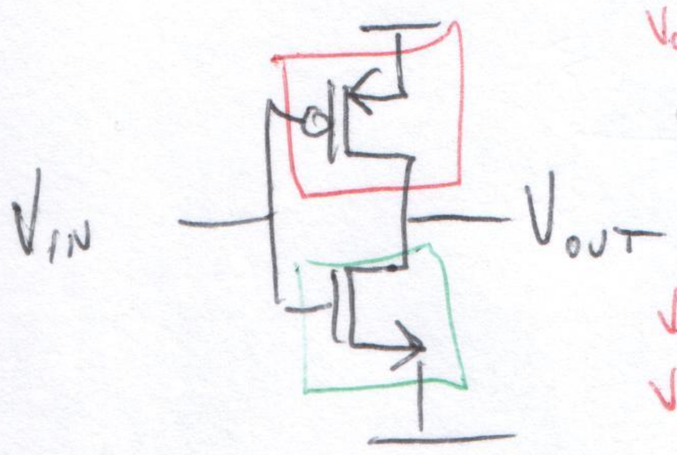
← same $K_p \frac{W}{L}$ as last NMOS inv.

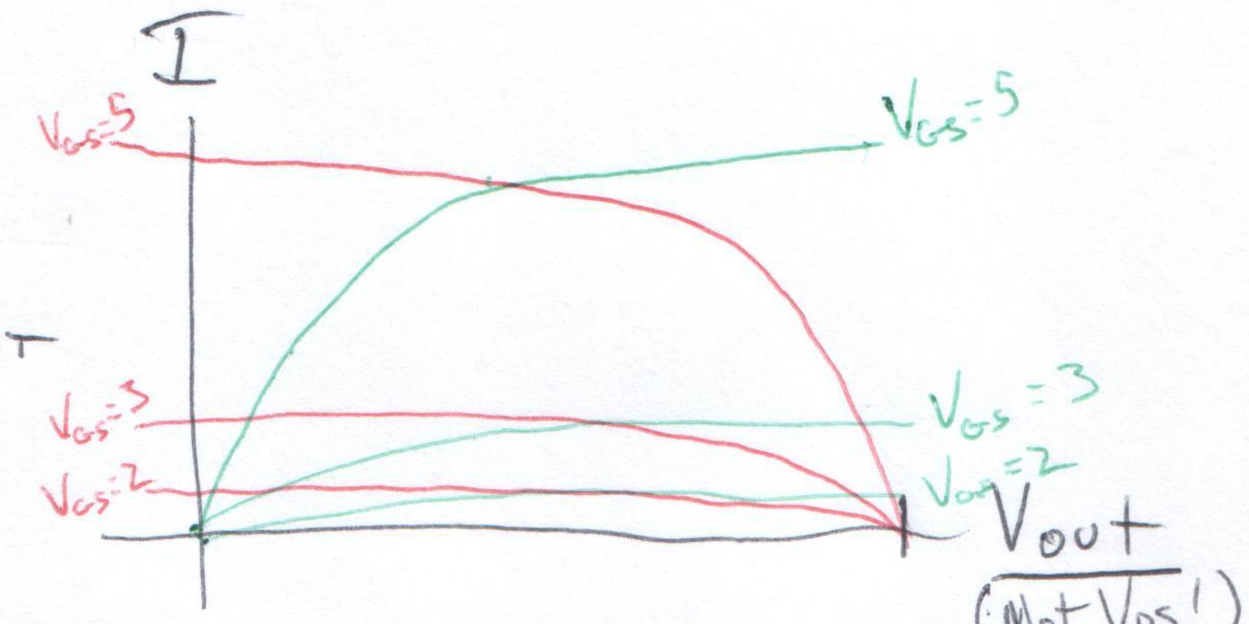




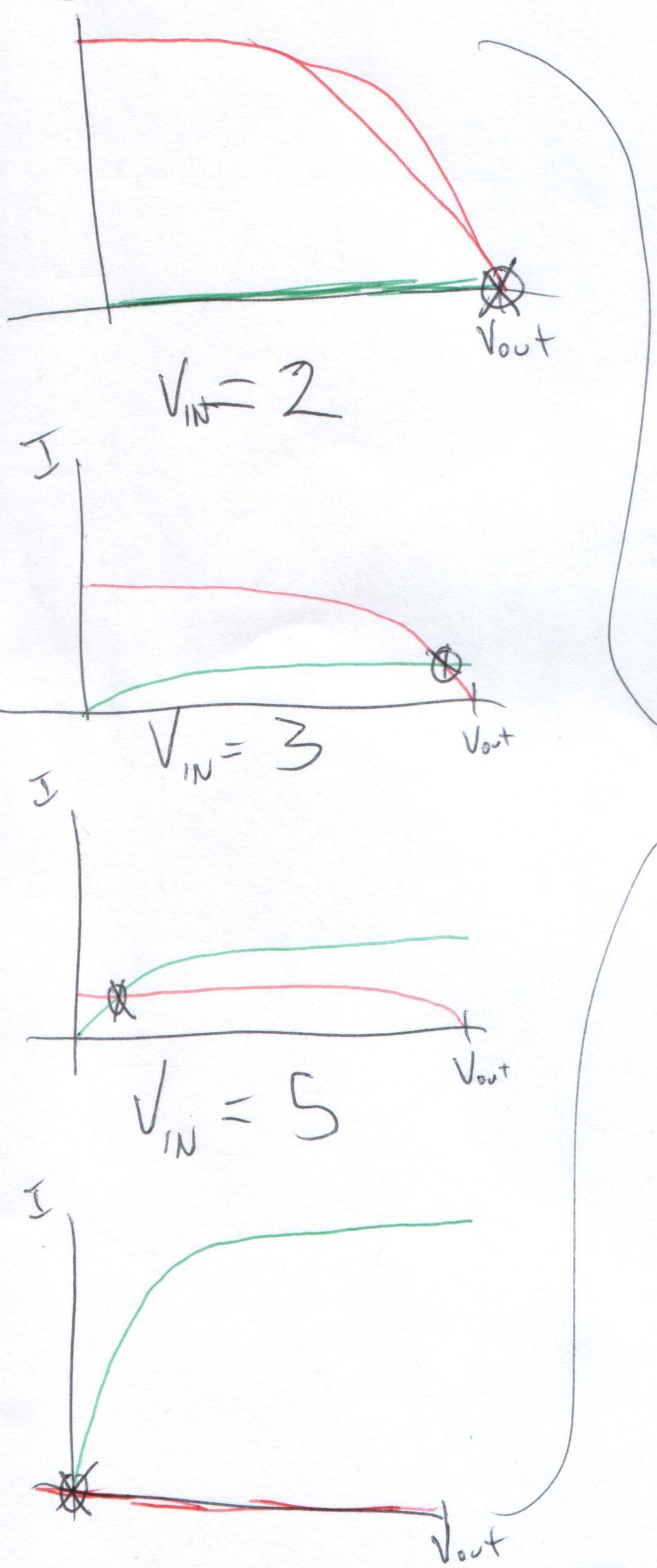


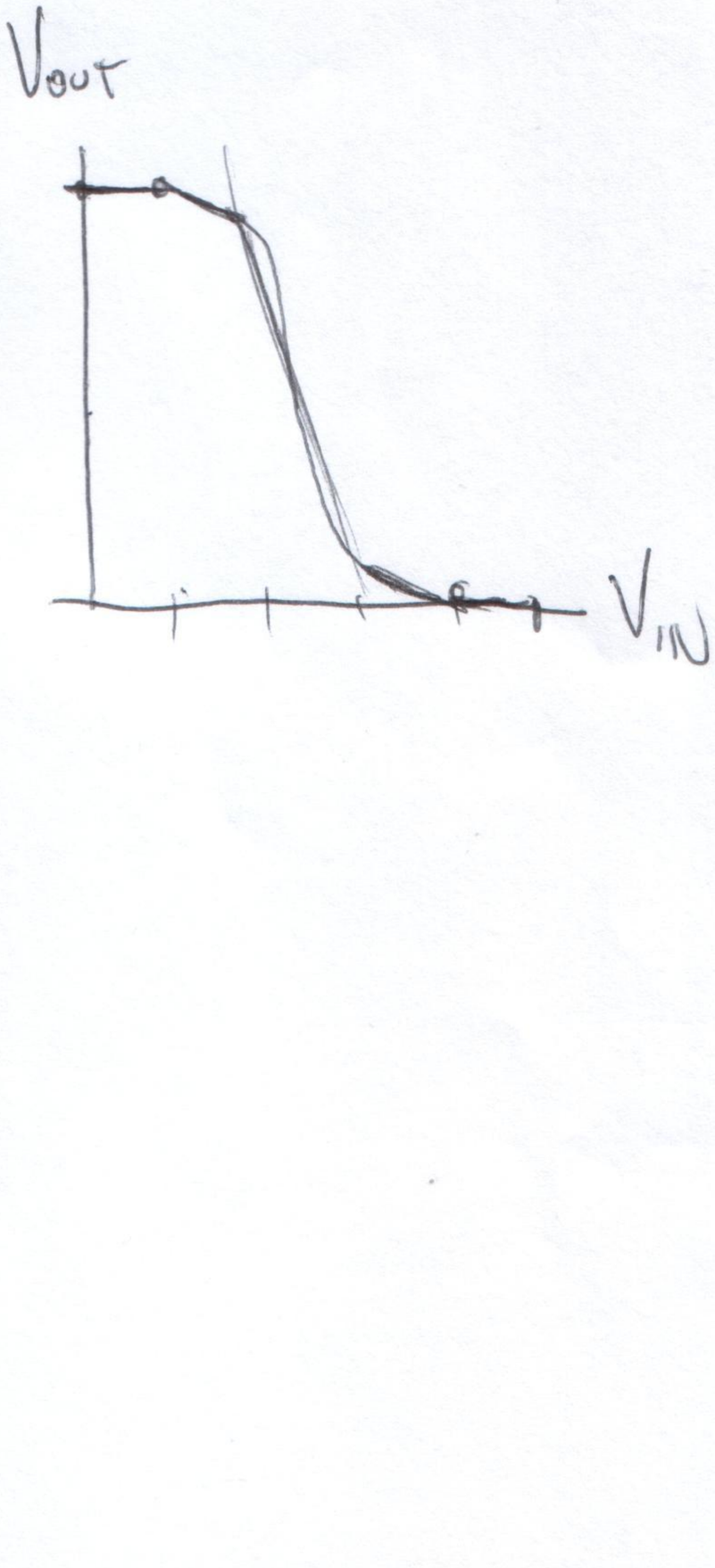
CMOS:





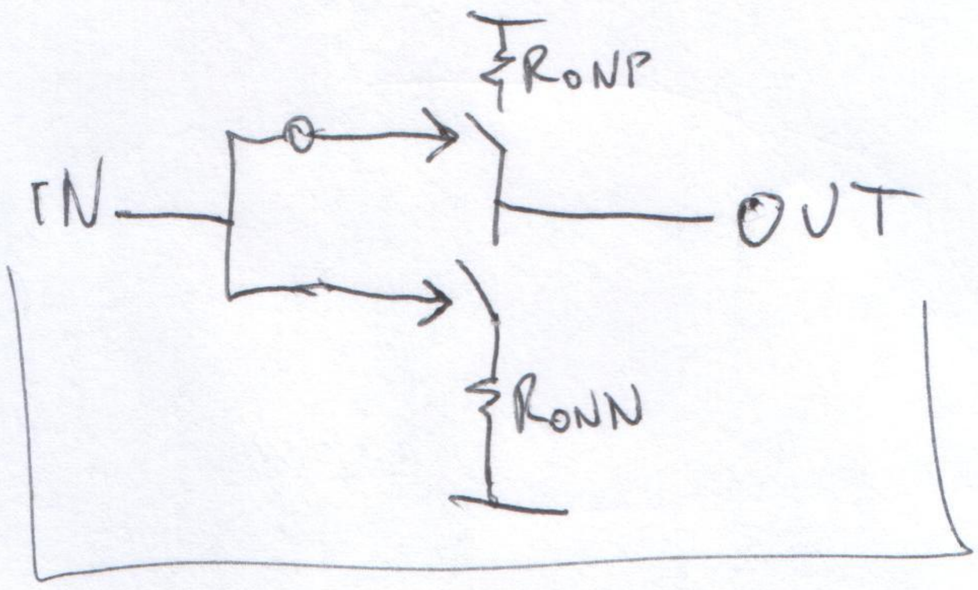
NMOS FIRST





Note: I am aware this is revolting.
This is the analysis you do to get details about something you will usually lock in a box and try very hard to forget.

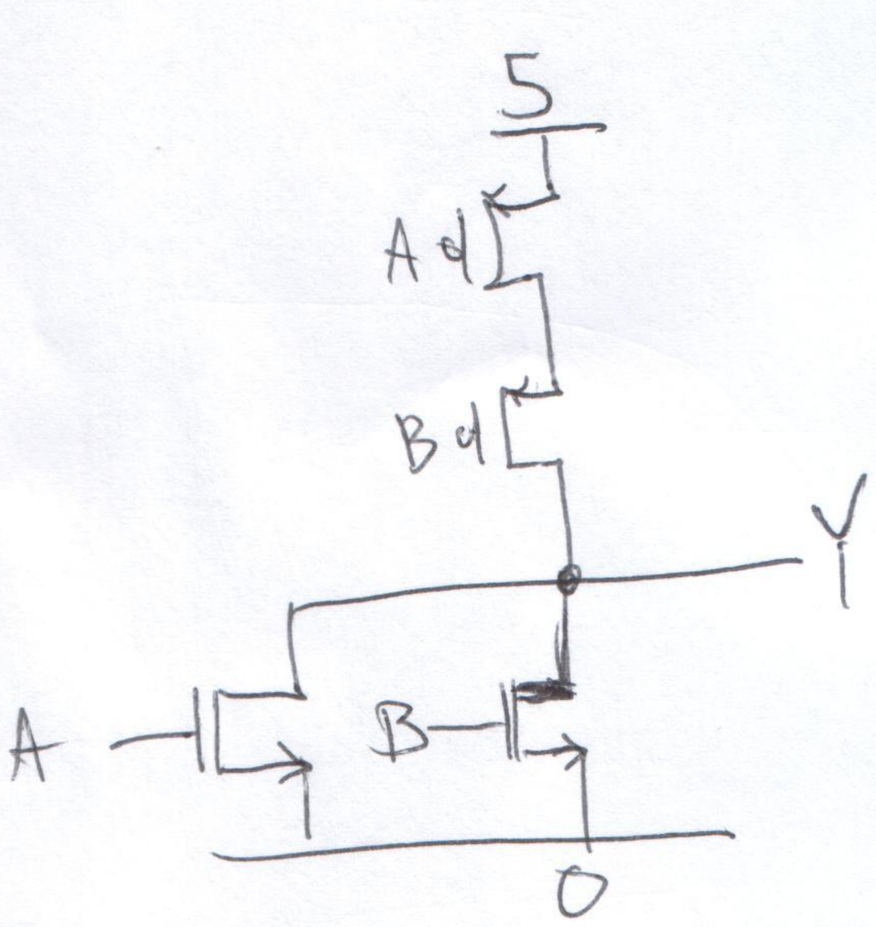
CMOS, as you will think of it from here out:



$$R_{ONP} \propto K_P' \frac{W_P}{L_P}$$

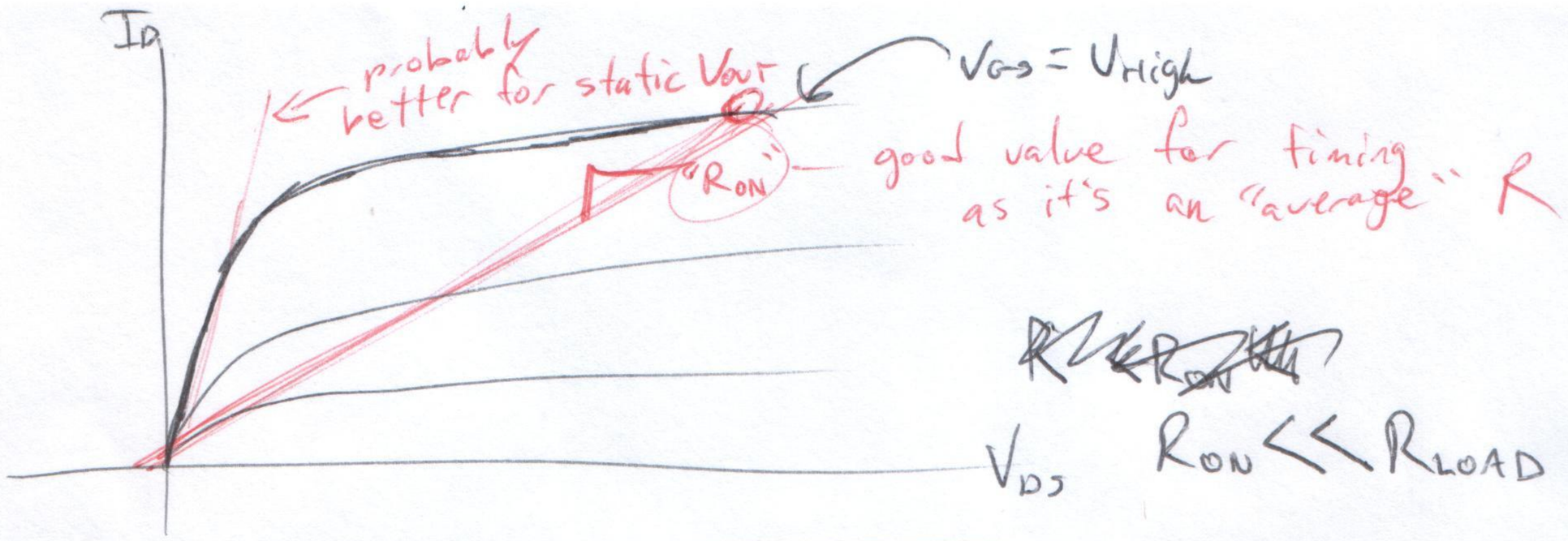
$$R_{ONN} \propto K_N' \frac{W_N}{L_N}$$

except for special cases where you will need an expert.

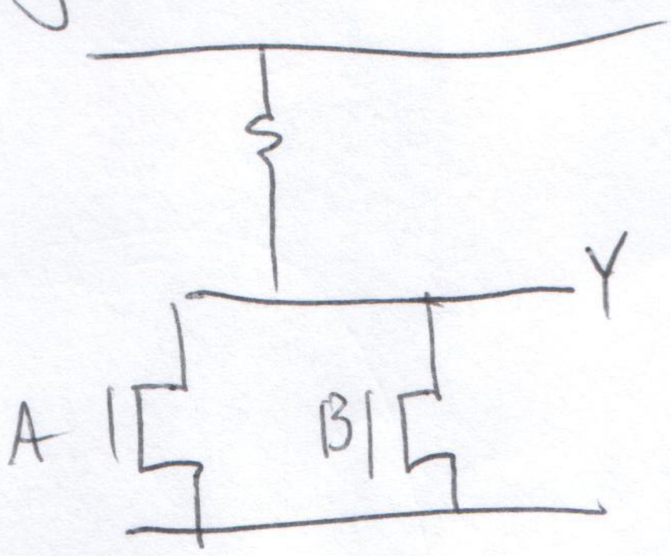


NOR

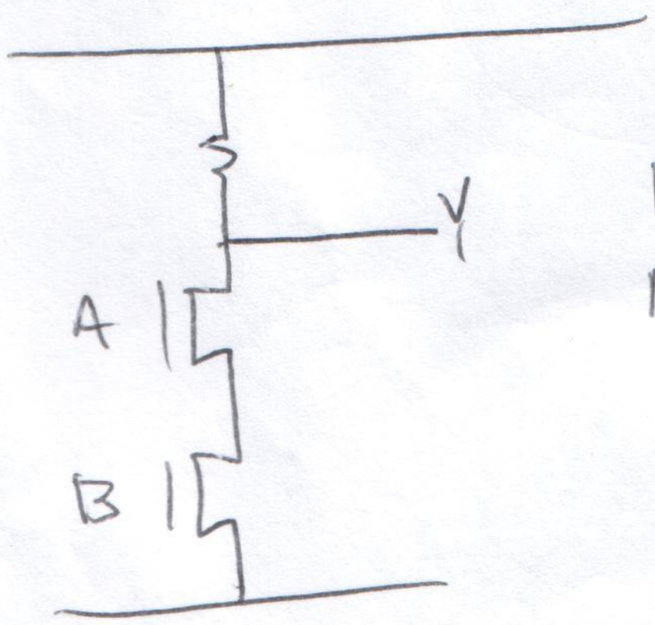
R_{ON}:



Logic:

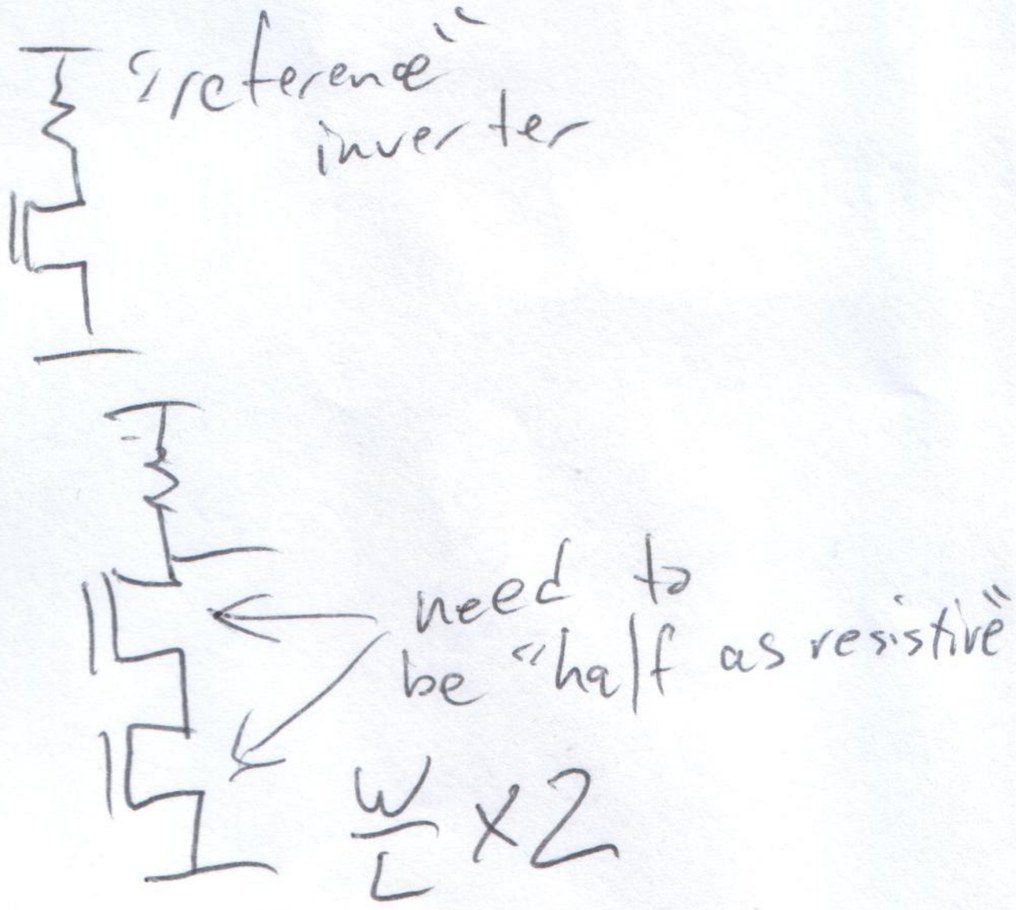


NOR
Not-OR



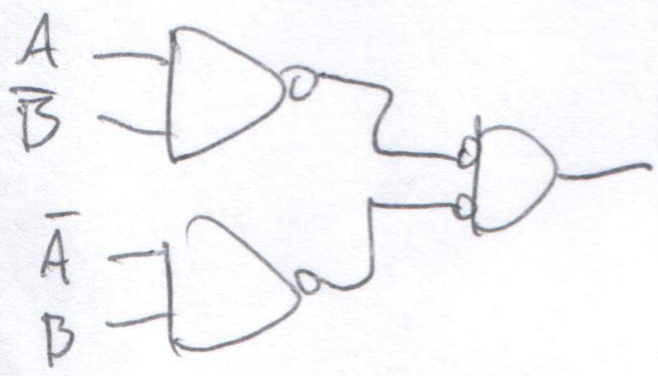
NAND
Not-And

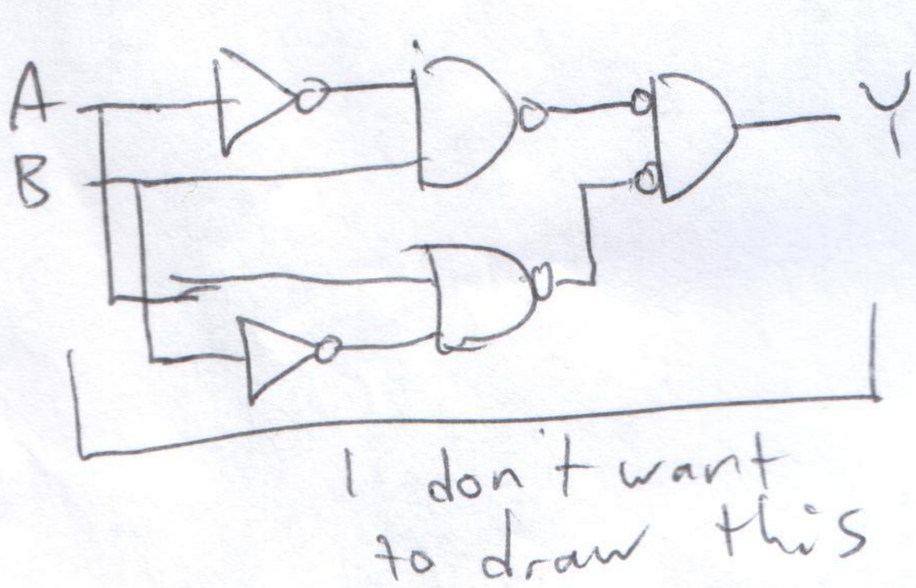
Delay design:

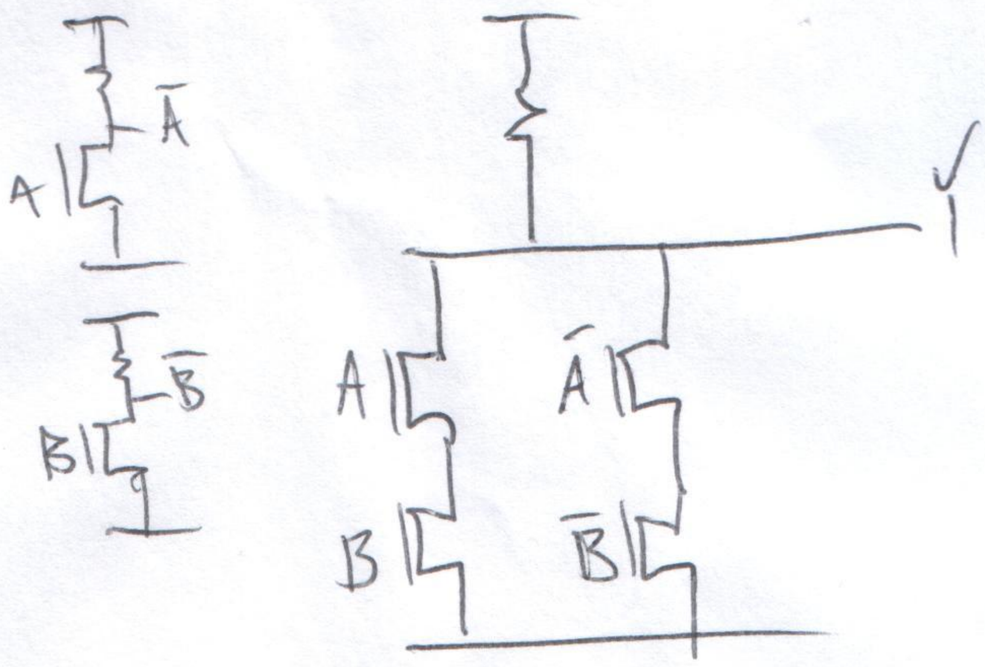


System Resources:

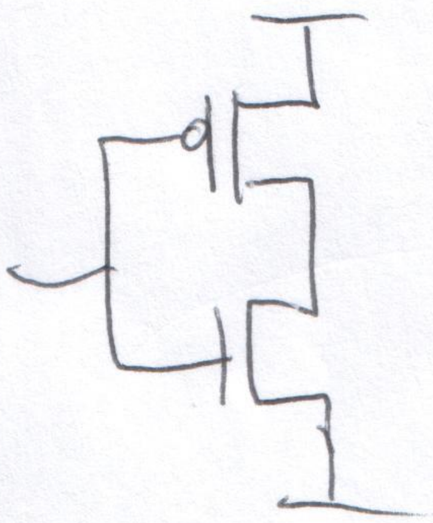
literally anything that concievably is needed by more than one thing

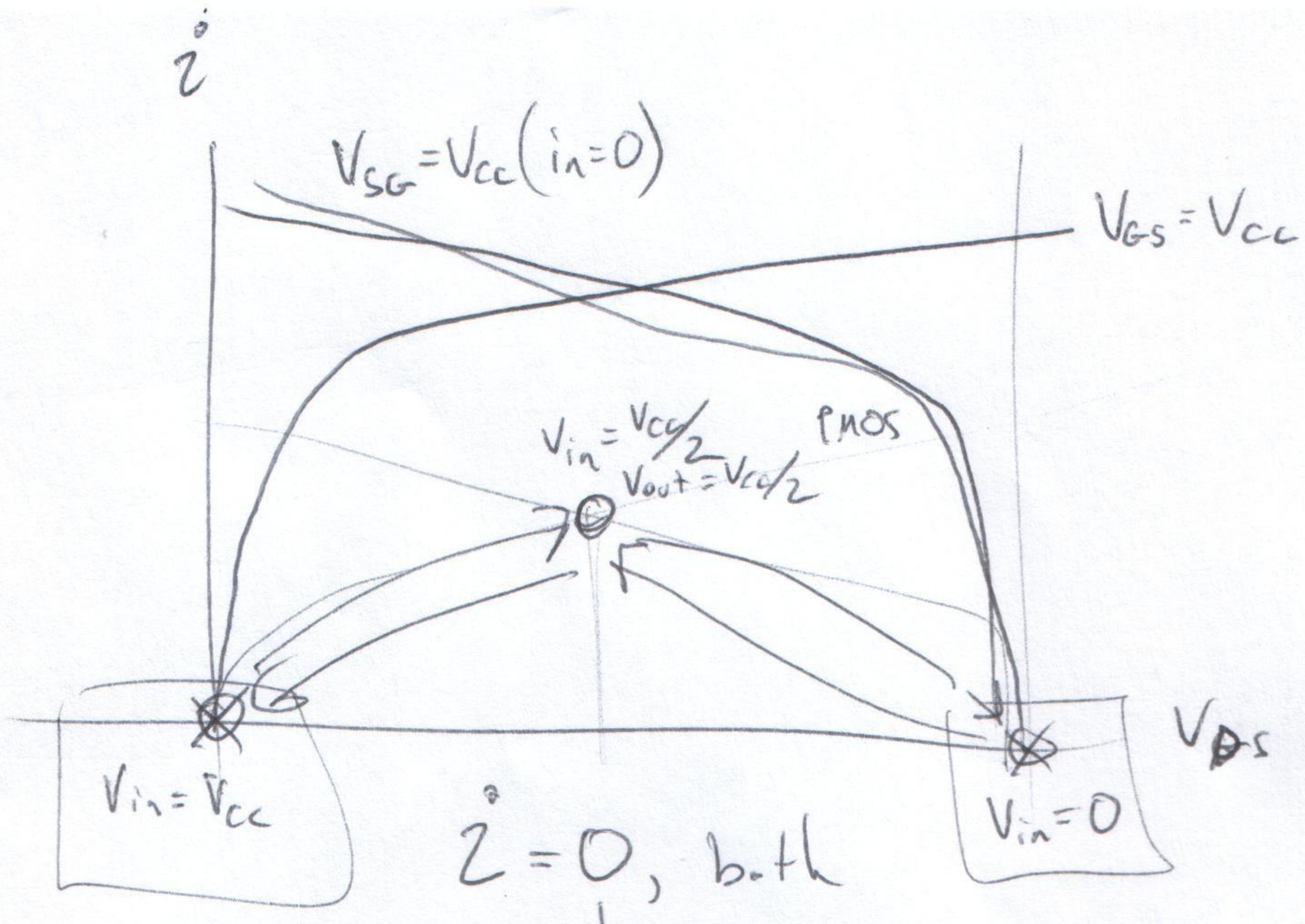




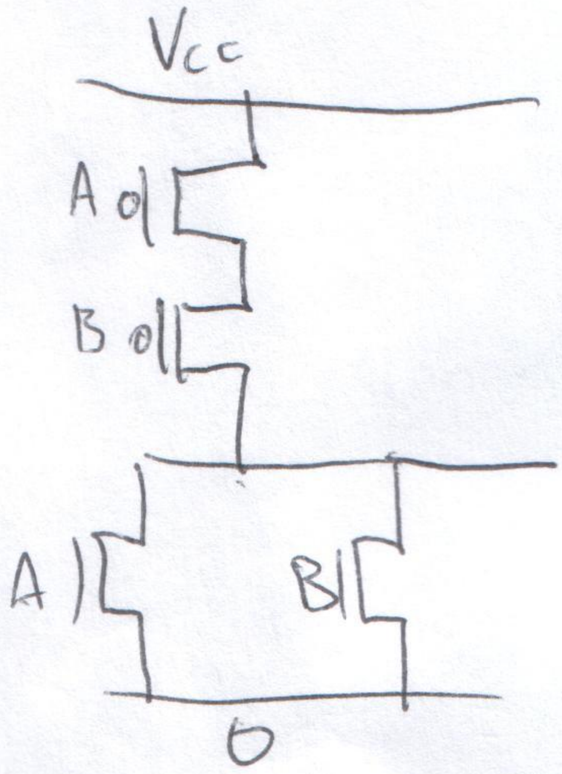


CMOS:

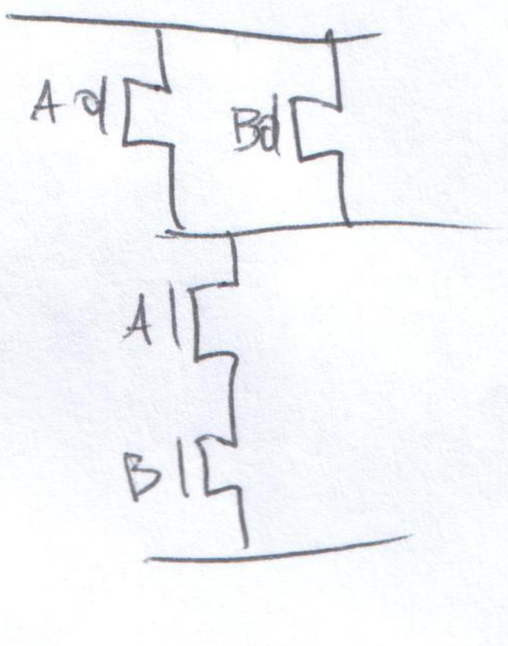




$i = 0$, both extremes

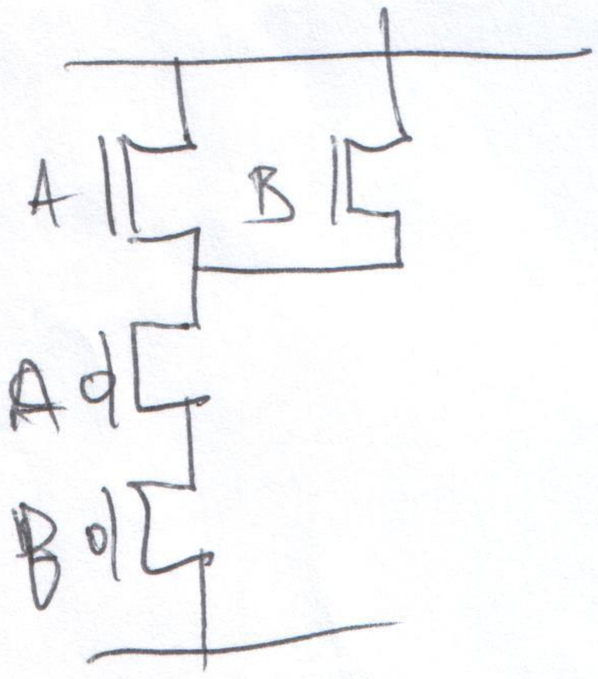


NOR

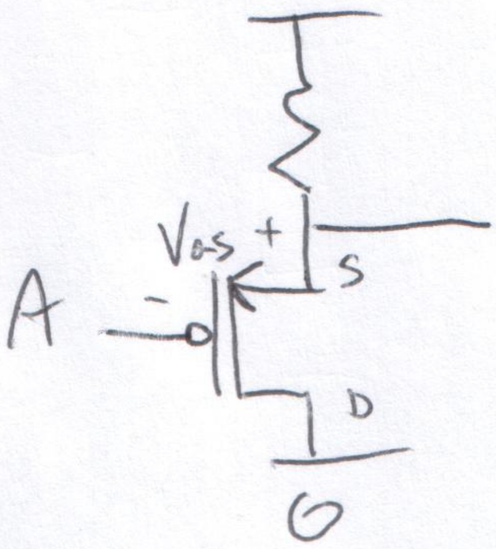


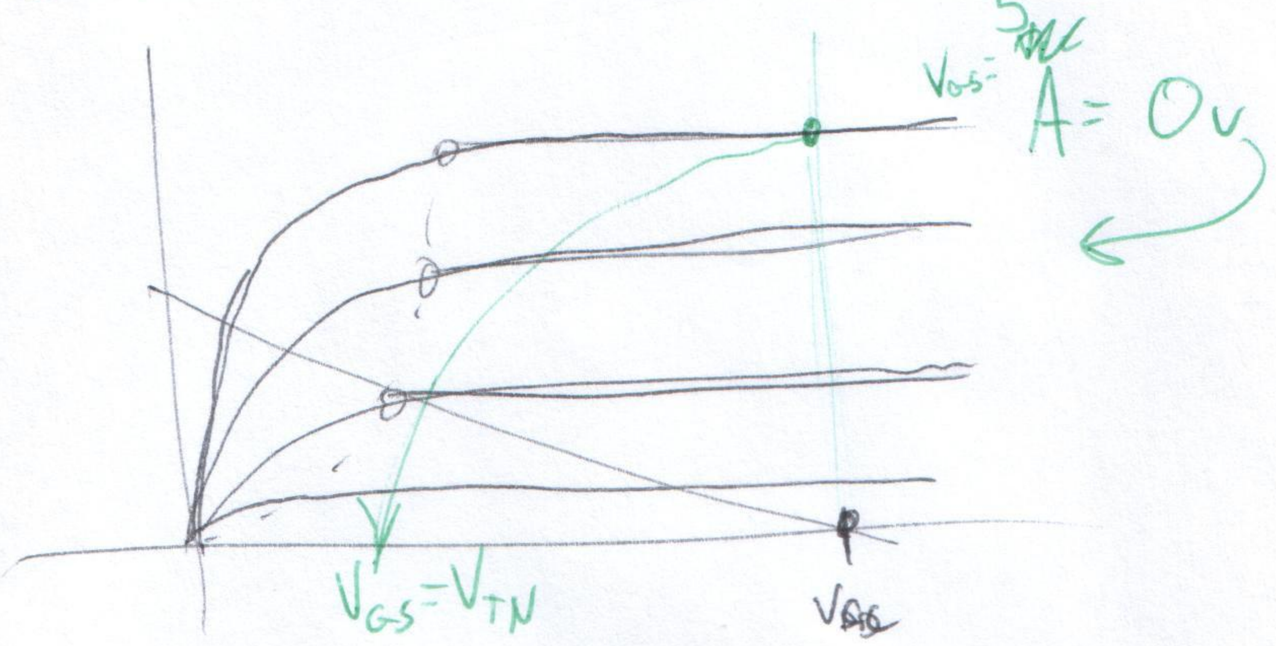
NAND

Why not do this?

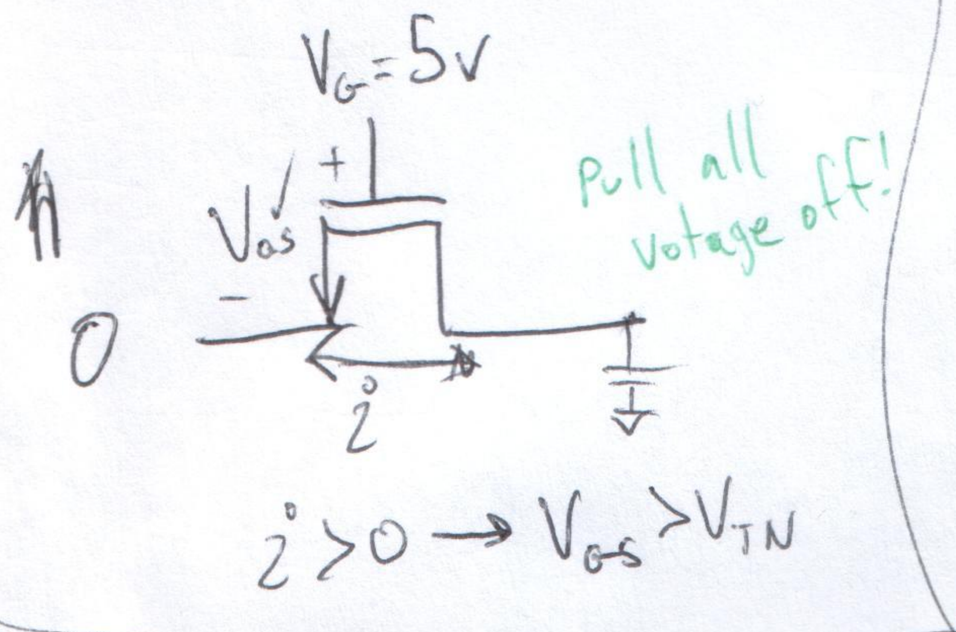


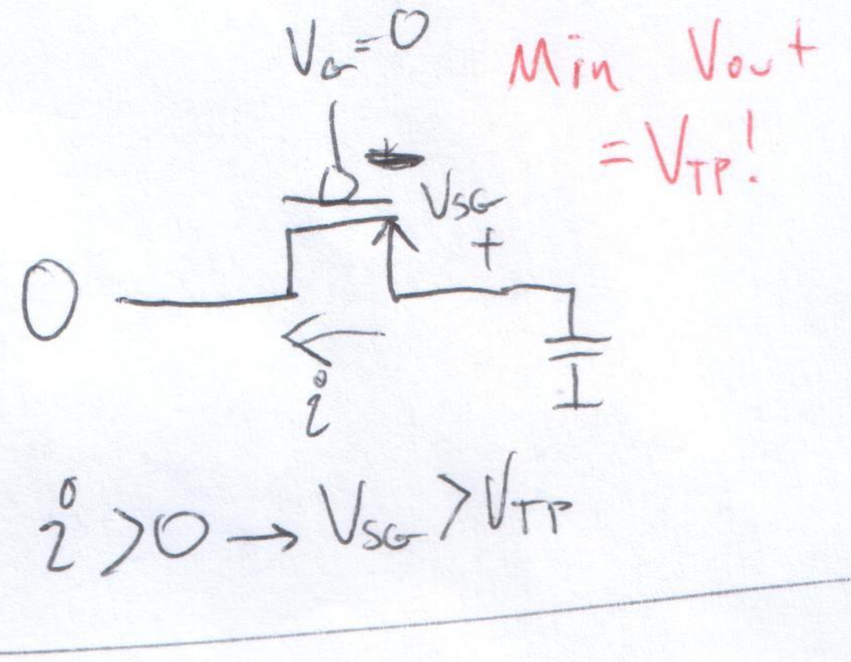
"PMOS Buffer"



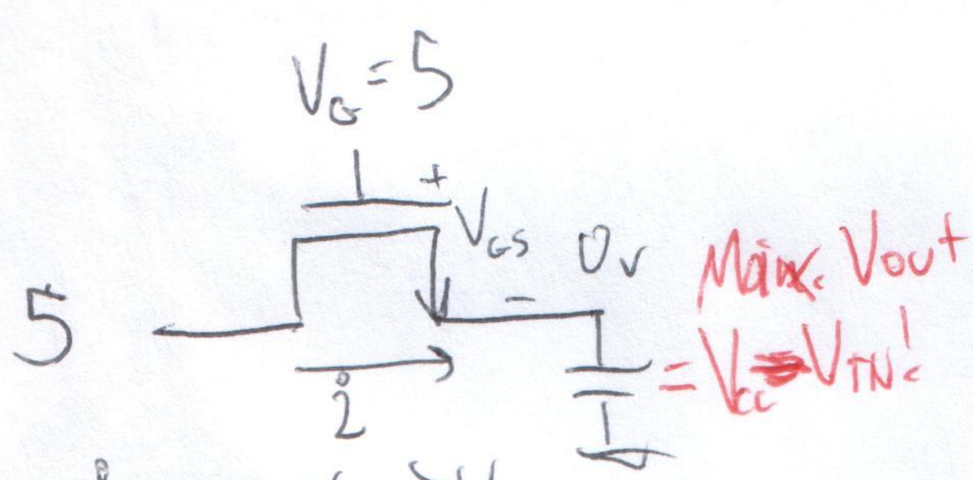


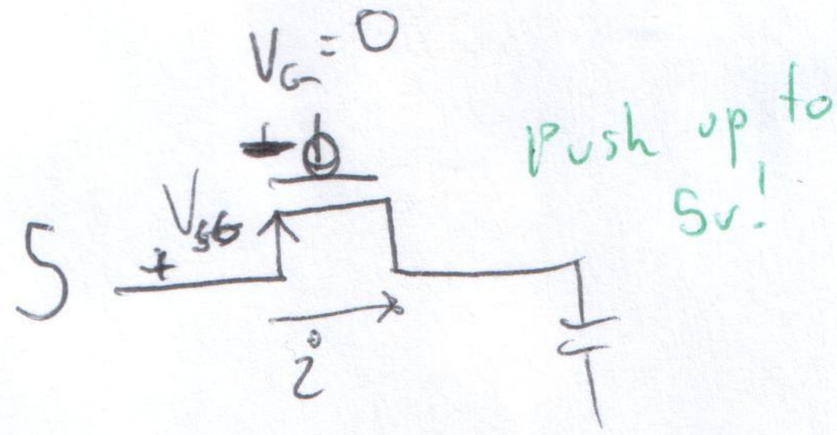
Pass 0





Pass 1





NMOS

PMOS

Implies design of T-Gate: